ML623 Virtex-6 FPGA GTX Transceiver Characterization Board

User Guide

UG724 (v1.1) September 15, 2010

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/30/10	1.0	Initial Xilinx release.
09/15/10	1.1	Added information about the Intersil power module to the paragraphs under GTX Transceiver Power Module, page 13, and to Table 1-2. Corrected sequence of P and N suffixes to Table 1-18 starting on FPGA pin T31 and ending on pin W27.

Table of Contents

About This Guide

This document describes the basic setup, features, and operation of the ML623 Virtex-6 FPGA GTX transceiver characterization board. The ML623 board provides the hardware environment for characterizing and evaluating the GTX transceivers available on the Virtex®-6 XC6VLX240T-2FFG1156C FPGA.

Guide Contents

This user guide contains the following chapters and appendices:

- Chapter 1, ML623 Board Features and Operation, describes the components, features, and operation of the ML623 Virtex-6 FPGA GTX transceiver characterization board.
- Appendix A, Default Jumper Positions, lists the jumpers that must be installed on the board for proper operation.
- Appendix B, VITA 57.1 FMC HPC Connector Pinout, provides a pinout reference for the FPGA mezzanine card (FMC) connector.
- Appendix C, ML623 Master UCF Listing, provides a listing of the ML623 master user constraints file (UCF).
- Appendix D, References, provides a list of references and links to related documentation.

To find additional documentation, see the Xilinx website at:

http://www.xilinx.com/support/documentation/index.htm.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

http://www.xilinx.com/support.

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
`Courier font`	Messages, prompts, and program files that the system displays	`speed grade: - 100`
`Courier bold`	Literal commands that you enter in a syntactical statement	**`ngdbuild`** *design_name*
Helvetica bold	Commands that you select from a menu	**File → Open**
	Keyboard shortcuts	**Ctrl+C**
Italic font	Variables in a syntax statement for which you must supply values	**`ngdbuild`** *design_name*
	References to other manuals	See the *Command Line Tools User Guide* for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Resources" for details. Refer to "Title Formats" in Chapter 1 for details.
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

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Chapter 1

ML623 Board Features and Operation

This chapter describes the components, features, and operation of the ML623 Virtex-6 FPGA GTX transceiver characterization board. The ML623 board provides the hardware environment for characterizing and evaluating the GTX transceivers available on the Virtex®-6 XC6VLX240T-2FFG1156C FPGA.

ML623 Board Features

- Virtex-6 XC6VLX240T-2FFG1156C FPGA
- On-board power supplies for all necessary voltages
- Power supply jacks for optional use of external power supplies
- JTAG configuration port for use with Platform Cable USB or Parallel Cable III/IV cables
- System ACE™ controller
- Power module supporting all Virtex-6 FPGA GTX transceiver power requirements
- A fixed, 200 MHz 2.5V LVDS oscillator wired to global clock inputs
- Two single-ended global clock inputs with SMA connectors
- Two pairs of differential global clock inputs with SMA connectors
- SuperClock-2 module supporting multiple frequencies
- 40 pairs of SMA connectors for the GTX transceivers
- 10 differential SMA connector pairs for the GTX transceiver clock inputs
- Power status LEDs
- General purpose DIP switches, LEDs, push buttons, and test I/O
- Three VITA 57.1 FMC HPC connectors
- System Monitor interface
- USB to UART bridge
- I^2C bus

The ML623 board block diagram is shown in Figure 1-1.

Caution! The ML623 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.

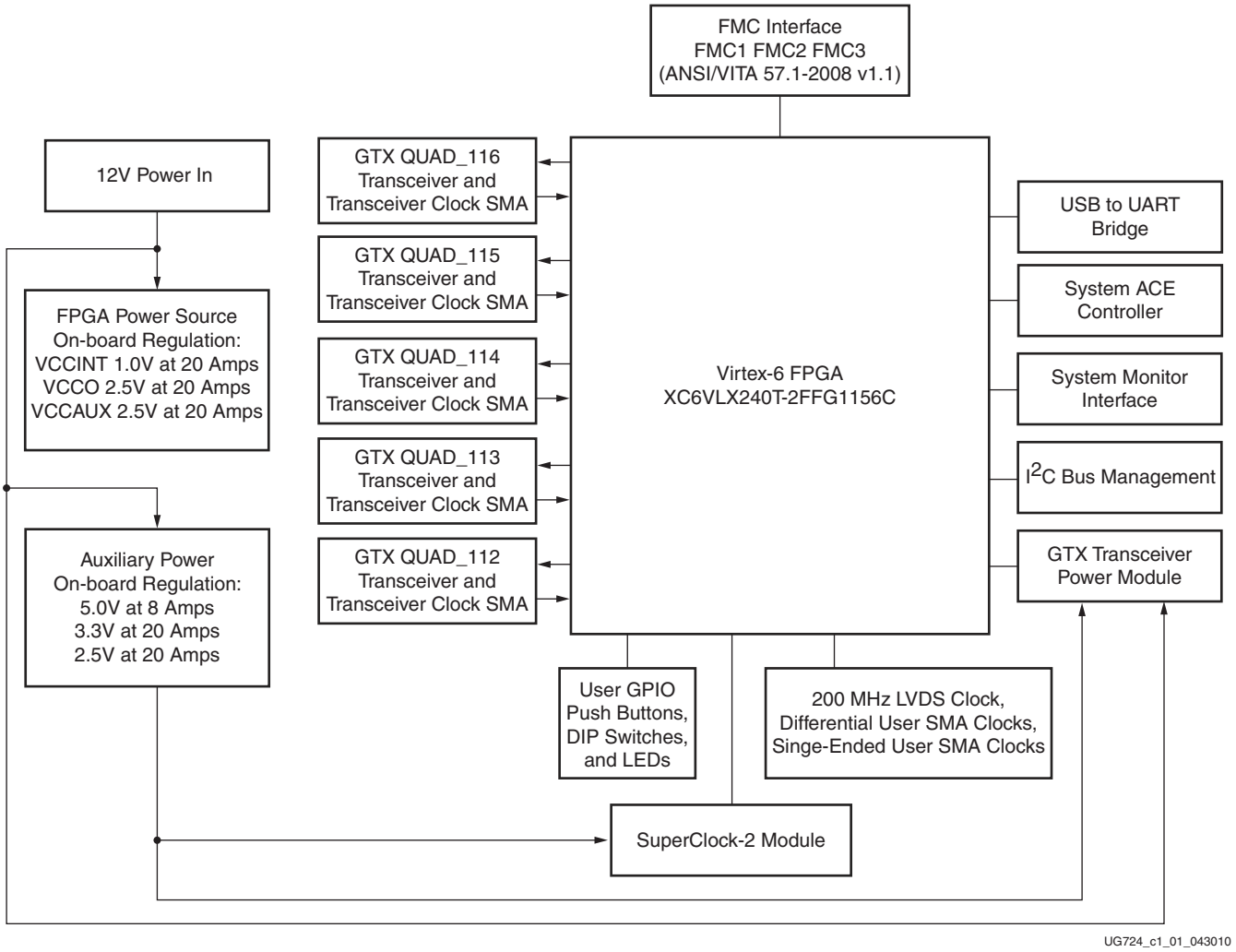
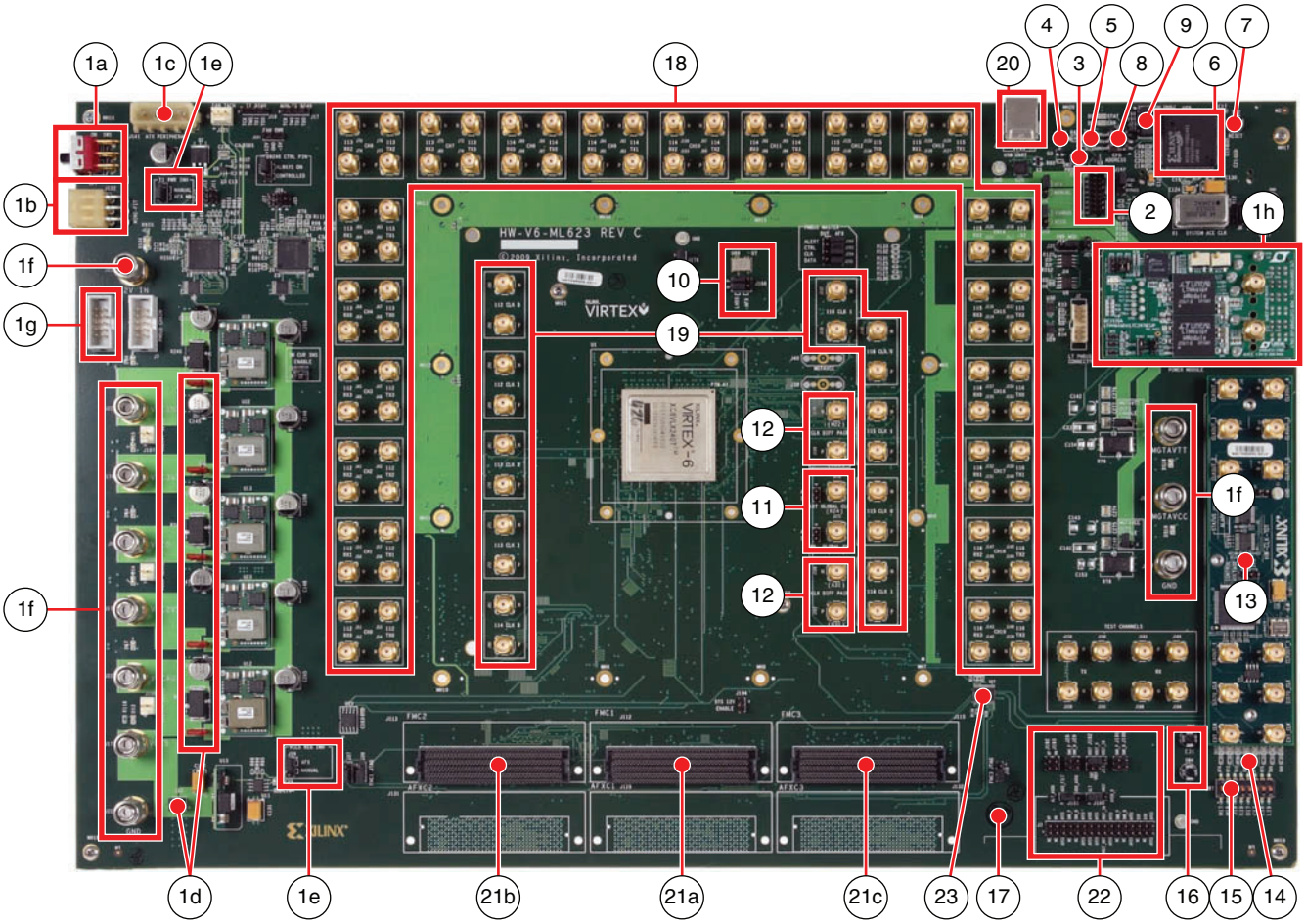


Figure 1-1: **ML623 Board Block Diagram**

Detailed Description

Figure 1-2 shows the ML623 board described in this user guide. Each numbered feature that is referenced in Figure 1-2 is described in the sections that follow.

Note: The image in Figure 1-2 is for reference only and might not reflect the current revision of the board.



1a	Main Power Switch (SW1)	10	200 MHz 2.5V LVDS oscillator (U7)
1b	12V Mini-Fit connector (J122)	11	Single-ended SMA global clock input (J171, J172)
1c	12V ATX connector (J141)	12	Differential SMA global clock inputs (J167, J166, J169, J170)
1d	Power regulation jumpers (J30, J31, J33, J102, J104, J105)	13	SuperClock-2 module
1e	Regulation Inhibit (J14, J19)	14	User LEDs, active High (DS10 - DS17)
1f	External power supply jacks	15	User DIP switches, active High (SW7)
1g	TI PMBus connector (J6)	16	User push buttons, active High (SW4, SW6)
1h	GTX Transceiver power supply module	17	User test I/O (J197)
2	FPGA configuration connector (J1)	18	GTX transceiver pins
3	PROG push button, active Low (SW5)	19	GTX transceiver clock input SMAs
4	DONE LED (DS6)	20	USB to UART bridge (U26)
5	INIT LED (DS20)	21a	FMC1 connector (J112)
6	System ACE controller (U25)	21b	FMC2 connector (J113)
7	System ACE reset, active Low (SW2)	21c	FMC3 connector (J115)
8	Configuration address DIP switch (SW3)	22	System Monitor
9	JTAG isolation jumpers (J22, J23, J195, J196)	23	I^2C Bus Management (U27)

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Figure 1-2: **Detailed Description of ML623 Board Components**

Power Management

Numbers 1a through 1h refer to the callouts in Figure 1-2:

1a: Main power switch (SW1)

1b: 12V Mini-Fit connector (J122)

1c: 12V ATX connector (J141)

1d: Power regulation jumpers (J30, J31, J33, J102, J104, J105)

1e: Regulation inhibit (J14, J19)

1f: External power supply jacks (J98, J173, J174, J175, J177, J178, J189, J220, J223, J227, J234)

1g: TI PMBus cable connector (J6)

1h: GTX transceiver power supply module

Board Power and Switch

The ML623 board is powered through J122 using the 12V AC adapter included with the board. J122 is a 6-pin (2 x 3) right angle Mini-Fit type connector.

Power can also be provided through:

- Connector J141 which accepts an ATX hard disk 4-pin power plug
- Jack J234 which can be used to connect to a bench-top power supply

Caution! Do NOT plug a PC ATX power supply 6-pin connector into J122 on the ML623 board. The ATX 6-pin connector has a different pinout than J122. Connecting an ATX 6-pin connector into J122 will damage the ML623 board and void the board warranty.

Caution! Do NOT apply power to J122 and connectors J141 and/or J234 at the same time. Doing so will damage the ML623 board.

The ML623 board power is turned on or off by switch SW1. When the switch is in the ON position, power is applied to the board and a green LED (DS36) illuminates.

Onboard Power Regulation

Figure 1-3 shows the onboard power supply architecture.

Note: Power regulation jumpers are not shown in Figure 1-3.

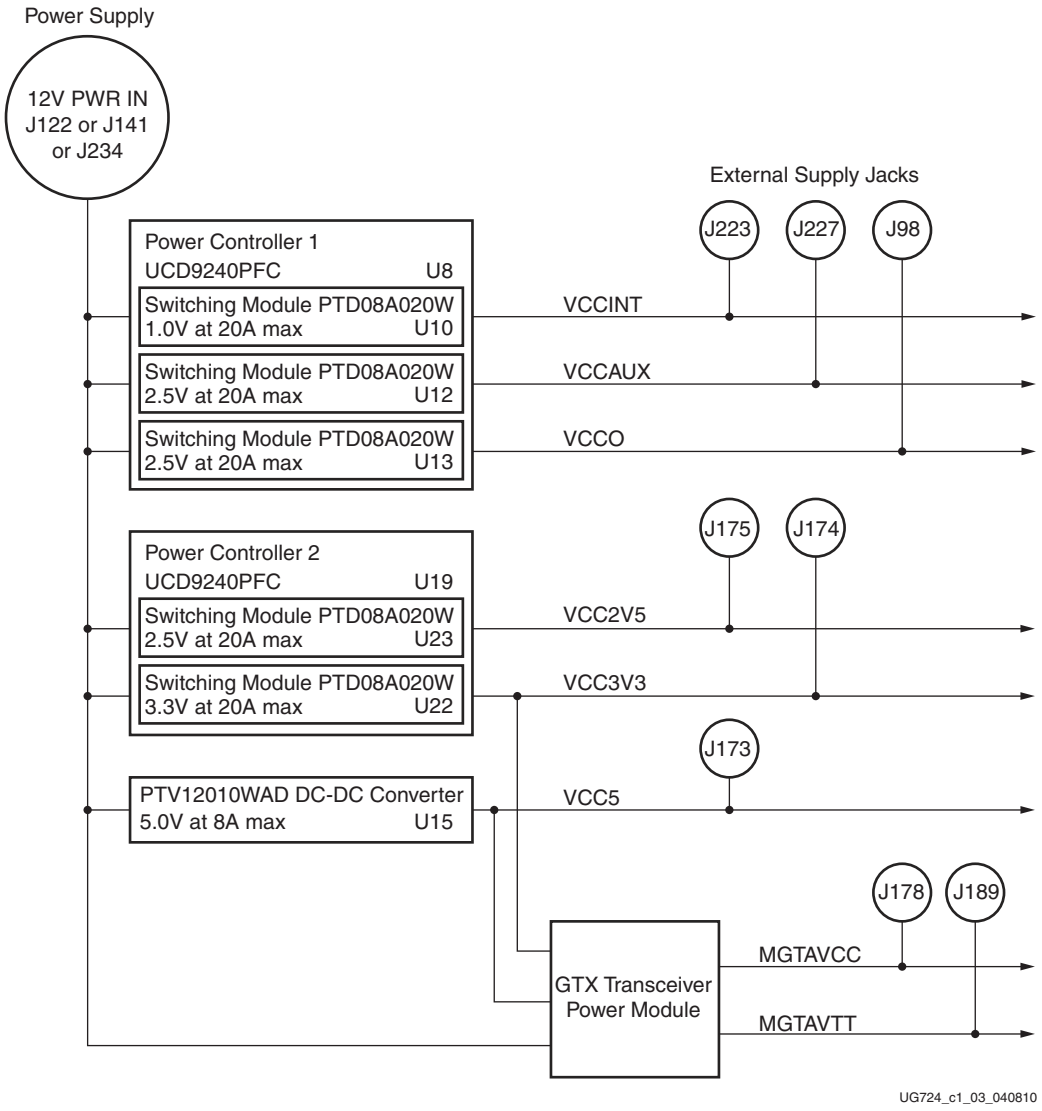

Figure 1-3: **ML623 Board Power Supply Block Diagram**

The ML623 board uses power regulators and PMBus compliant digital PWM system controllers from Texas Instruments to supply the core and auxiliary voltages listed in Table 1-1. The board can also be configured to use external bench power supply for each voltage. See Using External Power Sources.

Table 1-1: **Onboard Power System Devices**

Device	Reference Designator	Description	Power Rail Net Name	Typical Voltage	Power Regulation Jumper	External Supply Jack
Core voltage controller and regulators						
UCD9240PFC	U8	PMBus compliant digital PWM system controller (address = 52)				
PTD08A020W	U10	Adjustable switching regulator 20A, 0.6V to 3.6V	VCCINT	1.0V	J102	J223
PTD08A020W	U12	Adjustable switching regulator 20A, 0.6Vto 3.6V	VCCAUX	2.5V	J104	J227
PTD08A020W	U13	Adjustable switching regulator 20A, 0.6V to 3.6V	VCCO	2.5V	J105	J98
Auxiliary voltage controller and regulators						
UCD9240PFC	U19	PMBus compliant digital PWM system controller (address = 53)				
PTD08A020W	U23	Adjustable switching regulator 20A, 0.6V to 3.6V	VCC2V5	2.5V	J31	J175
PTD08A020W	U22	Adjustable switching regulator 20A, 0.6V to 3.6V	VCC3V3	3.3V	J30	J174
5V auxiliary power						
PTV12010WAD	U15	Adjustable switching regulator 8A, 1.2V to 5.5V	VCC5	5.0V	J33	J173

Using External Power Sources

The maximum output current rating for each power regulator is listed in Table 1-1. If a design exceeds this value on any power rail, power for that rail must be supplied through the external power jack using a supply capable of providing the required current.

Each power rail has a corresponding jack and jumper that is used to supply voltage to the rail using an external power supply. The jack, jumper, and regulator for each power rail is listed in Table 1-1.

> ***Caution!*** The power regulation jumper must be removed before applying external power to the power rail through its corresponding supply jack.

Disabling Onboard Power

Voltage regulators U10, U12, U13, U22, and U23 are disabled by installing a jumper across pins 2–3 of header J14. Voltage regulator U15 is disabled by installing a jumper across pins 2–3 of header J19.

Default Jumper Positions

A list of shunts and shorting plugs and their required positions for normal board operation is provided in Appendix A, Default Jumper Positions.

Monitoring Voltage and Current

Voltage and current monitoring and control are available for selected power rails through Texas Instruments' Fusion Digital Power graphical user interface (GUI). Both onboard TI power controllers are wired to the same PMBus. The PMBus connector, J6, is provided for use with the TI USB Interface Adapter PMBus pod and associated TI GUI.

References

More information about the power system components used by the ML623 board are available from the Texas Instruments digital power website at:

http://www.ti.com/ww/en/analog/digital-power/index.html

GTX Transceiver Power Module

The GTX transceiver power module supplies MGTAVCC and MGTAVTT voltages to the FPGA GTX transceivers. Three power modules are provided with the ML623 board. Any one of the three modules can be plugged into connectors J34 and J179 in the outlined and labeled power module location shown in Figure 1-4.

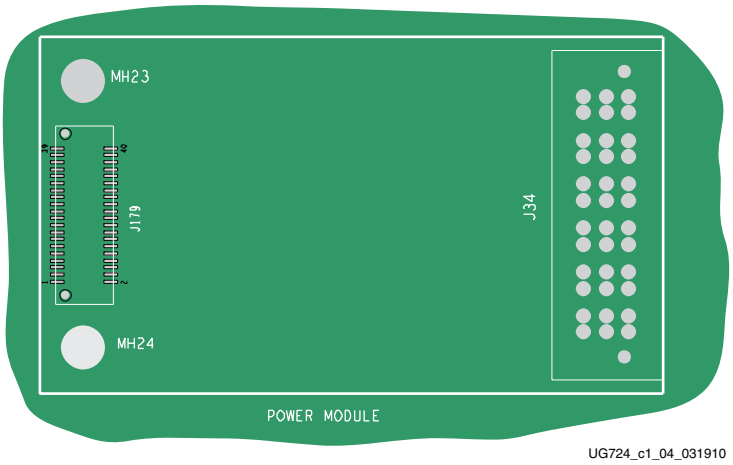

Figure 1-4: **Mounting Location, GTX Transceiver Power Module**

Table 1-2 describes the nominal voltage values for the MGTAVCC and MGTAVTT power rails. It also lists the maximum current ratings for each rail supplied by either module included with the ML623 board.

Table 1-2: **GTX Transceiver Power Module**

Power Supply Rail Net Name	Typical Voltage	Maximum Current Rating			Regulation Jumper			External Supply Jack
		Linear Technology Module	Texas Instruments Module	Intersil Module	Linear Technology Module	Texas Instruments Module	Intersil Module	
MGTAVCC	1.025V	20A	10A	10A	JP1	N/A	N/A	J178
MGTAVTT	1.2V	12A	6A	6A	JP2	N/A	N/A	J189

The GTX transceiver power rails also have corresponding input voltage jacks to supply each voltage independently from a bench-top power supply (See External Supply Jack column in Table 1-2). To supply power externally to one or both rails when the Linear

Technology Module is installed, place jumpers on JP1 and/or JP2 across pins 2–3 (OFF position).

Note: The power regulation jumper must be placed in the OFF position before connecting an external supply to its corresponding supply jack.

The Texas Instruments and Intersil modules do not have voltage regulation jumpers and *must* be removed from the board before providing external power to the GTX transceiver rails.

Caution! The Intersil module features an MGTAVCC voltage adjust header, J1. Make sure to remove any jumper across J1 before powering the board with the Intersil module installed. Failure to do so may damage the FPGA.

FPGA Configuration

[Figure 1-2, callout 2]

The FPGA is configured in JTAG mode only using one of the following options:

- Platform Cable USB
- Parallel Cable IV
- Parallel Cable III
- System ACE controller

Detailed information on the System ACE controller is available in DS080, *System ACE CompactFlash Solution*.

The FPGA is configured through one of the aforementioned cables by connecting the cable to the download cable connector, J1.

The FPGA is configured through the System ACE controller by setting the 3-bit configuration address DIP switches (SW3) to select one of eight bitstreams stored on a CompactFlash memory card (see Configuration Address DIP Switches, page 16).

Note: The System ACE controller is bypassed when the flying wire leads or the Parallel Cable IV cable is used, causing no disruption in the JTAG chain.

The JTAG chain of the board is illustrated in Figure 1-5 (the four System ACE interface isolation jumpers described in JTAG Isolation Jumpers are not shown). Shorting pins 1–2 on header J162 automatically bypasses the FMC modules and the GTX transceiver power supply module in the chain.

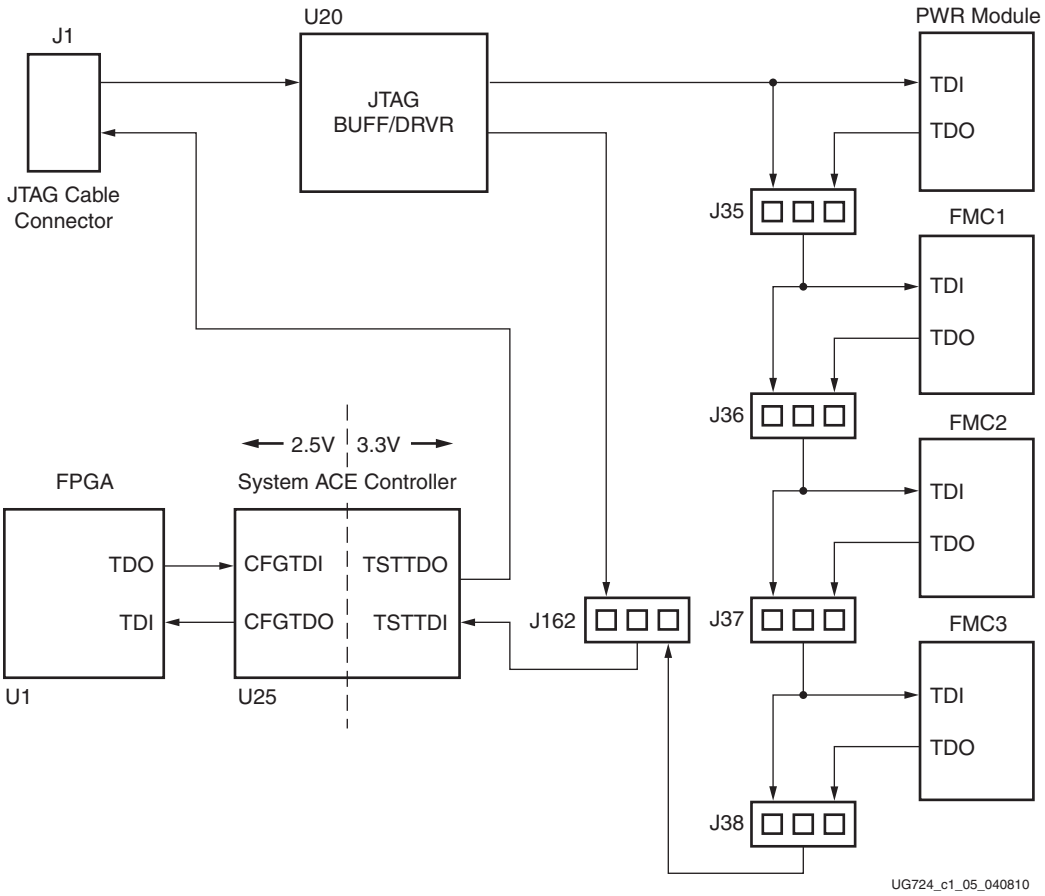

Figure 1-5: **JTAG Chain**

PROG Push Button

[Figure 1-2, callout 3]

Pressing the PROG push button (SW5) grounds the active-Low program pin of the FPGA.

DONE LED

[Figure 1-2, callout 4]

The DONE LED (DS6) indicates the state of the DONE pin of the FPGA. When the DONE pin is High, DS6 lights indicating the FPGA is successfully configured.

INIT LED

[Figure 1-2, callout 5]

The INIT LED (DS20) lights during FPGA initialization.

System ACE Controller

[Figure 1-2, callout 6]

The onboard System ACE controller (U25) allows storage of multiple configuration files on a CompactFlash card. These configuration files can be used to program the FPGA. The CompactFlash card connects to the CompactFlash card connector (U24) located directly below the System ACE controller on the back side of the board.

System ACE Controller Reset

[Figure 1-2, callout 7]

Pressing push button SW2 (RESET) resets the System ACE controller. Reset is an active-Low input.

Configuration Address DIP Switches

[Figure 1-2, callout 8]

DIP switch SW3 selects one of the eight configuration bitstream addresses in the CompactFlash memory card. The switch settings for selecting each address are shown in Table 1-3.

Table 1-3: **SW3 DIP Switch Configuration**

Address	ADR2	ADR1	ADR0
0	O(1)	O	O
1	O	O	C(2)
2	O	C	O
3	O	C	C
4	C	O	O
5	C	O	C
6	C	C	O
7	C	C	C

Notes:

1. O indicates the open switch position (logic 0).
2. C indicates the closed switch position (logic 1).

JTAG Isolation Jumpers

[Figure 1-2, callout 9]

The group of four 2-pin headers shown in Figure 1-6 provide the option to isolate the FPGA JTAG interface from the System ACE controller by removing the shunts from all four headers. The FPGA JTAG interface can also be driven directly from these headers by attaching the flying wire JTAG cable to pin 2 of each header. Figure 1-6 shows a more detailed representation of the isolation jumpers as part of the broader JTAG chain in Figure 1-5.

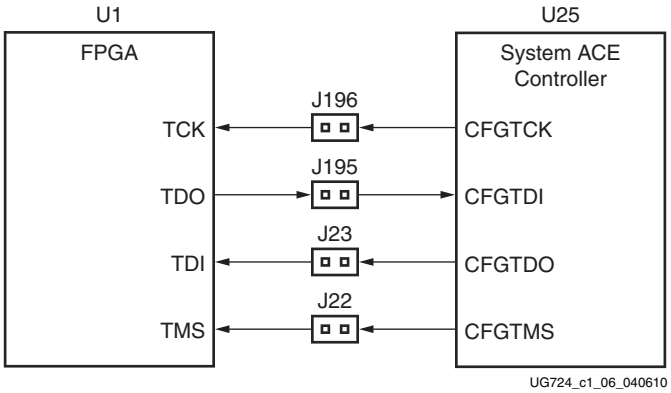

Figure 1-6: **JTAG Isolation Jumpers**

Table 1-4 indicates the FPGA pin name associated with each jumper.

Table 1-4: **JTAG Isolation Jumpers**

Reference Designator	FPGA Pin Name
J22	TMS
J23	TDI
J195	TDO
J196	TCK

200 MHz 2.5V LVDS Oscillator

[Figure 1-2, callout 10]

The ML623 board has one 2.5V LVDS differential 200 MHz oscillator (U7) connected to the FPGA global clock inputs. Table 1-5 lists the FPGA pin connections to the LVDS oscillator. The 200 MHz differential clock is enabled by placing two shunts (P, N) across J188 header pins 1–3 and 2–4 (LVDS).

Table 1-5: **LVDS Oscillator Global Clock Connections**

FPGA Pin	Net Name	U7 Pin
J9	IO_LVDS_CLK_P	4
H9	IO_LVDS_CLK_N	5

Single-Ended SMA Global Clock Inputs

[Figure 1-2, callout 11]

The ML623 board provides two single-ended clock input SMA connectors that can be used for connecting to an external function generator. The FPGA clock pins are connected to the SMA connectors as shown in Table 1-6.

To use these clock inputs, remove jumpers across AFX SEL headers J186 and J187.

Table 1-6: **Single-Ended SMA Clock Connections**

FPGA Pin	Net Name	SMA Connector
H28	CLK_A	J171
K24	CLK_B	J172

Differential SMA Global Clock Inputs

[Figure 1-2, callout 12]

The ML623 board provides two pairs of differential SMA transceiver clock inputs that can be used for connecting to an external function generator. The FPGA clock pins are connected to the SMA connectors as shown in Table 1-7.

Table 1-7: **Differential SMA Clock Connections**

FPGA Pin	Net Name	SMA Connector
B31	CLK_DIFF_A_P	J167
A31	CLK_DIFF_A_N	J168
L23	CLK_DIFF_B_P	J169
M22	CLK_DIFF_B_N	J170

SuperClock-2 Module

[Figure 1-2, callout 13]

The SuperClock-2 module connects to the clock module interface connector (J32) and provides a programmable, low-noise clock source for the ML623 board. The clock module maps to FPGA I/O by way of 24 control pins, 3 LVDS pairs, 1 regional clock pair, and 1 reset pin. Table 1-8 shows the FPGA I/O mapping for the SuperClock-2 module interface. The ML623 board also supplies 5V, 3.3V, and 2.5V input power to the clock module interface.

Table 1-8: **SuperClock-2 FPGA I/O Mapping**

FPGA Pin	Net Name	J32 Pin
J17	CM_LVDS1_P	1
J16	CM_LVDS1_N	3
K18	CM_LVDS2_P	9
K17	CM_LVDS2_N	11
E16	CM_LVDS3_P	17
D16	CM_LVDS3_N	19
A16	CM_GCLK_P	25
B16	CM_GCLK_N	27
C18	CM_CTRL_0	61
B18	CM_CTRL_1	63

Table 1-8: **SuperClock-2 FPGA I/O Mapping *(Cont'd)***

FPGA Pin	Net Name	J32 Pin
K22	CM_CTRL_2	65
K21	CM_CTRL_3	67
A19	CM_CTRL_4	69
A18	CM_CTRL_5	71
J22	CM_CTRL_6	73
H22	CM_CTRL_7	75
D19	CM_CTRL_8	77
E19	CM_CTRL_9	79
E21	CM_CTRL_10	81
D21	CM_CTRL_11	83
H20	CM_CTRL_12	85
H19	CM_CTRL_13	87
A20	CM_CTRL_14	89
E23	CM_CTRL_15	91
E22	CM_CTRL_16	93
B22	CM_CTRL_17	95
B21	CM_CTRL_18	97
J21	CM_CTRL_19	99
J20	CM_CTRL_20	101
C23	CM_CTRL_21	103
B23	CM_CTRL_22	105
G22	CM_CTRL_23	107
G21	CM_RST	66

User LEDs (Active High)

[Figure 1-2, callout 14]

DS10 through DS17 are eight active-High LEDs that are connected to user I/O pins on the FPGA as shown in Table 1-9. These LEDs can be used to indicate status or any other purpose determined by the user.

Table 1-9: **User LEDs**

FPGA Pin	Net Name	Reference Designator
M15	LED1	DS17
M16	LED2	DS16

Table 1-9: **User LEDs *(Cont'd)***

FPGA Pin	Net Name	Reference Designator
F15	LED3	DS15
G15	LED4	DS14
B15	LED5	DS13
A15	LED6	DS12
G16	LED7	DS11
F16	LED8	DS10

User DIP Switches (Active High)

[Figure 1-2, callout 15]

The DIP switch SW7 provides a set of eight active-High switches that are connected to user I/O pins on the FPGA as shown in Table 1-10. These pins can be used to set control pins or any other purpose determined by the user.

Table 1-10: **User DIP Switches**

FPGA Pin	Net Name	Reference Designator
M17	SW1	SW7
M18	SW2	
J19	SW3	
K19	SW4	
B17	SW5	
C17	SW6	
L18	SW7	
L19	SW8	

User Push Buttons (Active High)

[Figure 1-2, callout 16]

SW5 and SW6 are active-High user push buttons that are connected to user I/O pins on the FPGA as shown in Table 1-11. These switches can be used for any purpose determined by the user.

Table 1-11: **User Push Buttons**

FPGA Pin	Net Name	Reference Designator
E31	PB_SW1	SW6
F31	PB_SW2	SW4

User Test I/O

[Figure 1-2, callout 17]

A standard 2 x 6, 100-mil pitch header (J197) brings out 6 FPGA I/O for test purposes. Table 1-12 lists these pins.

Table 1-12: **User Test I/O**

FPGA Pin	Net Name	J197 Pin
U30	IO_L8N_SRCC_14_U30	2
U31	IO_L8P_SRCC_14_U31	4
D32	IO_L15N_16_D32	6
D31	IO_L15P_16_D31	8
K27	IO_L9N_MRCC_16_K27	10
K26	IO_L9P_MRCC_16_K26	12

GTX Transceiver Pins

[Figure 1-2, callout 18]

All FPGA GTX transceiver pins are connected to differential SMA connector pairs. The GTX transceivers are grouped into five sets of four (referred to as *Quads)* which share two differential reference clock pin pairs (Figure 1-7). The transceiver pins and their corresponding SMA connector are shown in Table 1-13.

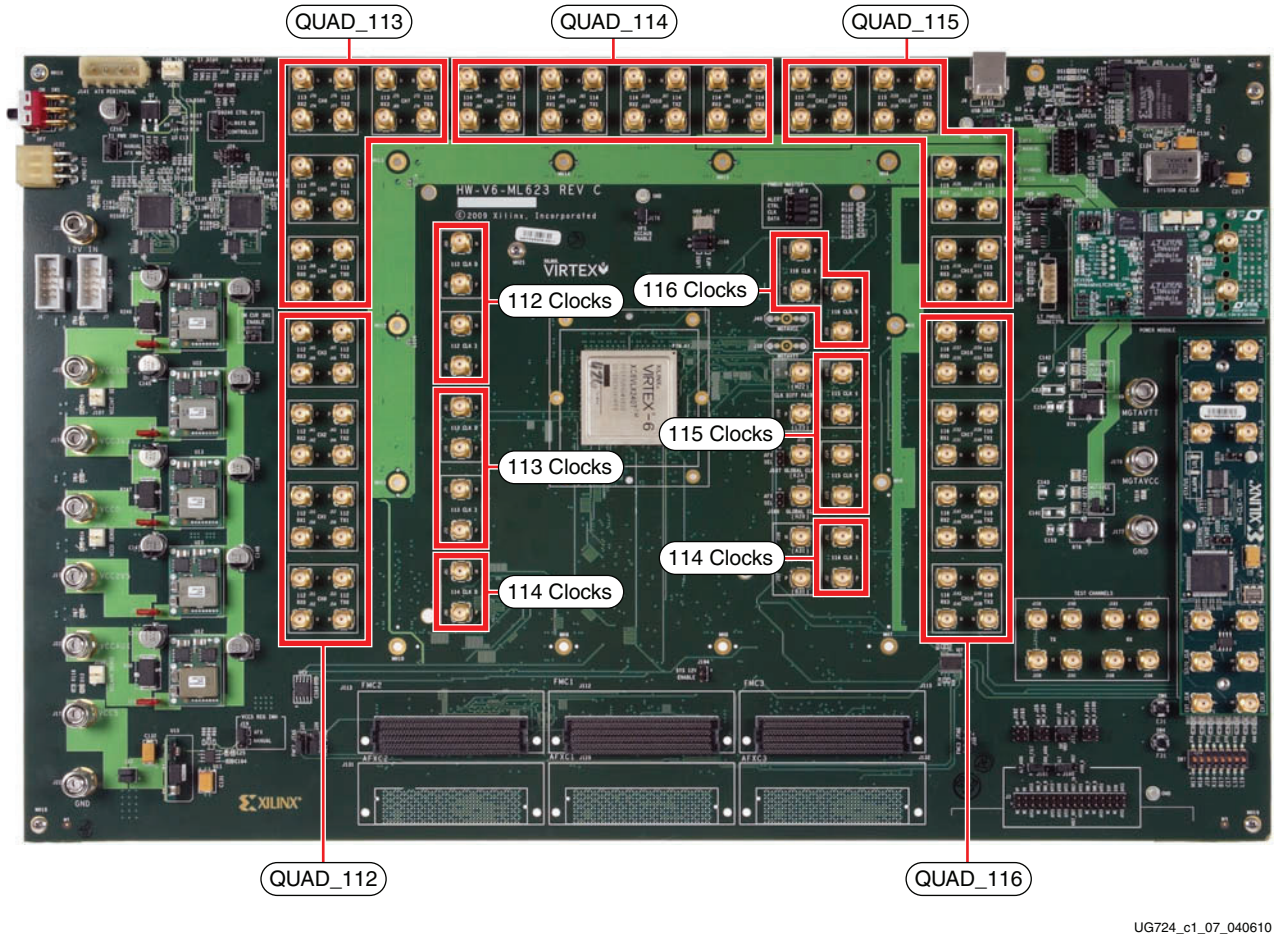

Figure 1-7: **GTX Transceiver and Reference Clock SMA Locations**

Table 1-13: **GTX Transceiver Pins**

FPGA Pin	Net Name	SMA Connector	Trace Length (Mils)
AP5	112_RX0_P	J51	7,365
AP6	112_RX0_N	J52	7,361
AP1	112_TX0_P	J53	9,861
AP2	112_TX0_N	J54	9,853
AM5	112_RX1_P	J55	6,449
AM6	112_RX1_N	J56	6,438
AN3	112_TX1_P	J57	9,079
AN4	112_TX1_N	J58	9,089
AL3	112_RX2_P	J41	5,624
AL4	112_RX2_N	J42	5,634

Table 1-13: **GTX Transceiver Pins *(Cont'd)***

FPGA Pin	Net Name	SMA Connector	Trace Length (Mils)
AM1	112_TX2_P	J43	8,185
AM2	112_TX2_N	J44	8,193
AJ3	112_RX3_P	J45	5,748
AJ4	112_RX3_N	J46	5,738
AK1	112_TX3_P	J47	7,348
AK2	112_TX3_N	J48	7,356
AG3	113_RX0_P	J68	6,550
AG4	113_RX0_N	J69	6,550
AH1	113_TX0_P	J67	6,722
AH2	113_TX0_N	J66	6,729
AF5	113_RX1_P	J65	7,531
AF6	113_RX1_N	J64	7,542
AF1	113_TX1_P	J63	6,520
AF2	113_TX1_N	J62	6,528
AE3	113_RX2_P	J79	8,300
AE4	113_RX2_N	J78	8,307
AD1	113_TX2_P	J77	7,553
AD2	113_TX2_N	J76	7,558
AC3	113_RX3_P	J80	7,166
AC4	113_RX3_N	J75	7,175
AB1	113_TX3_P	J74	6,595
AB2	113_TX3_N	J73	6,599
AA3	114_RX0_P	J88	6,112
AA4	114_RX0_N	J89	6,119
Y1	114_TX0_P	J87	5,441
Y2	114_TX0_N	J86	5,449
W3	114_RX1_P	J85	5,096
W4	114_RX1_N	J84	5,102
V1	114_TX1_P	J83	4,435
V2	114_TX1_N	J82	4,442
U3	114_RX2_P	J103	4,398
U4	114_RX2_N	J100	4,424
T1	114_TX2_P	J99	4,633

Table 1-13: **GTX Transceiver Pins *(Cont'd)***

FPGA Pin	Net Name	SMA Connector	Trace Length (Mils)
T2	114_TX2_N	J97	4,625
R3	114_RX3_P	J96	5,068
R4	114_RX3_N	J95	5,075
P1	114_TX3_P	J94	5,614
P2	114_TX3_N	J93	5,619
N3	115_RX0_P	J136	6,166
N4	115_RX0_N	J135	6,172
M1	115_TX0_P	J134	6,678
M2	115_TX0_N	J133	6,676
L3	115_RX1_P	J130	7,150
L4	115_RX1_N	J128	7,156
K1	115_TX1_P	J127	7,640
K2	115_TX1_N	J126	7,650
K5	115_RX2_P	J120	6,957
K6	115_RX2_N	J121	6,964
H1	115_TX2_P	J118	7,669
H2	115_TX2_N	J117	7,665
J3	115_RX3_P	J116	7,397
J4	115_RX3_N	J114	7,387
F1	115_TX3_P	J111	7,626
F2	115_TX3_N	J110	7,634
G3	116_RX0_P	J157	8,171
G4	116_RX0_N	J155	8,181
D1	116_TX0_P	J154	8,113
D2	116_TX0_N	J153	8,111
E3	116_RX1_P	J152	9,019
E4	116_RX1_N	J151	9,028
C3	116_TX1_P	J150	9,203
C4	116_TX1_N	J149	9,198
D5	116_RX2_P	J147	9,536
D6	116_RX2_N	J146	9,548
B1	116_TX2_P	J145	10,015
B2	116_TX2_N	J144	10,018

Table 1-13: **GTX Transceiver Pins *(Cont'd)***

FPGA Pin	Net Name	SMA Connector	Trace Length (Mils)
B5	116_RX3_P	J143	9,846
B6	116_RX3_N	J142	9,837
A3	116_TX3_P	J140	10,663
A4	116_TX3_N	J139	10,659

GTX Transceiver Clock Input SMAs

[Figure 1-2, callout 19]

The ML623 board provides differential SMA connectors that can be used for connecting an external function generator to all GTX transceiver reference clock inputs of the FPGA. The FPGA reference clock pins are connected to the SMA connectors as shown in Table 1-14.

Table 1-14: **GTX Transceiver Clock Inputs to the FPGA**

FPGA Pin	Net Name	SMA Connector
AK6	112_REFCLK0_P	J59
AK5	112_REFCLK0_N	J60
AH6	112_REFCLK1_P	J49
AH5	112_REFCLK1_N	J50
AD6	113_REFCLK0_P	J70
AD5	113_REFCLK0_N	J61
AB6	113_REFCLK1_P	J72
AB5	113_REFCLK1_N	J71
V6	114_REFCLK0_P	J90
V5	114_REFCLK0_N	J81
T6	114_REFCLK1_P	J92
T5	114_REFCLK1_N	J91
P6	115_REFCLK0_P	J125
P5	115_REFCLK0_N	J124
M6	115_REFCLK1_P	J123
M5	115_REFCLK1_N	J106
H6	116_REFCLK0_P	J156
H5	116_REFCLK0_N	J148
F6	116_REFCLK1_P	J138
F5	116_REFCLK1_N	J137

USB to UART Bridge

[Figure 1-2, callout 20]

Communications between the ML623 board and a host computer are through a USB cable connected to J9. Control is provided by U26, a USB to UART bridge (Silicon Laboratories CP2103). Table 1-15 lists the pin assignments and signals for the USB connector J9.

Table 1-15: **USB Type B Connector Pin Assignments and Signals**

J9 Pin	Signal Name	Description
1	VBUS	+5V from host system (not used)
2	USB_DATA_N	Bidirectional differential serial data (N-side)
3	USB_DATA_P	Bidirectional differential serial data (P-side)
4	GROUND	Signal ground

The CP2103 supports an IO voltage range of 1.8V to 2.5V on the ML623 board. The connections between the FPGA and CP2103 should use the LVCMOS25 IO standard. UART IP (for example, Xilinx® XPS UART Lite) must be implemented in the FPGA fabric. The FPGA supports the USB to UART bridge using four signal pins:

- Transmit (TX)
- Receive (RX)
- Request to Send (RTS)
- Clear to Send (CTS)

Connections of these signals between the FPGA and the CP2103 at U26 are listed in Table 1-16.

Table 1-16: **FPGA to U26 (CP2103 USB to UART Bridge) Connections**

FPGA Pin	FPGA Function	Net Name	U26 Pin	U26 Function
E32	RTS, output	USB_CTS	22	CTS, input
E33	CTS, input	USB_RTS	23	RTS, output
F30	TX, data out	USB_RX	24	RXD, data in
G30	RX, data in	USB_TX	25	TXD, data out

The bridge device also provides as many as 4 GPIO signals that can be defined by the user for status and control information (Table 1-17).

Table 1-17: **CP2103 USB to UART Bridge User GPIO**

FPGA Pin	Net Name	U26 Pin
J29	USB_GPIO0	19
K28	USB_GPIO1	18
B34	USB_GPIO2	17
C33	USB_GPIO3	16

A royalty-free software driver named Virtual COM Port (VCP) is available from Silicon Laboratories. This driver permits the CP2103 USB to UART bridge to appear as a COM

port to the host computer communications application software (for example, HyperTermimal or TeraTerm). The VCP driver must be installed on the host computer prior to establishing communications with the ML623 board.

FMC HPC Connectors

[Figure 1-2, callouts 21a, 21b, and 21c]

The ML623 board features three high pin count (HPC) connectors as defined by the VITA 57.1.1 FMC specification. The FMC HPC connector is a 10 x 40 position socket that is fully populated with 400 pins. See Appendix B, VITA 57.1 FMC HPC Connector Pinout, for a cross-reference of signal names to pin coordinates.

Each FMC HPC connector on the ML623 board provides connectivity for:

- 79 differential user-defined pairs:
  - 34 LA pairs
  - 23 HA pairs
  - 22 HB pairs
- 4 differential clocks

Note: The V_{ADJ} voltage for the FMC HPC connectors on the ML623 board is fixed at 2.5V (non-adjustable). The 2.5V rail cannot be turned off. The VITA 57.1 FMC interfaces on the ML623 board are compatible with 2.5V mezzanine cards capable of supporting 2.5V V_{ADJ}.

The FMC HPC connectors on the ML623 board are identified as: FMC1 at J112, FMC2 at J113, and FMC3 at J115. The connections for each of these connectors are listed in Table 1-18, Table 1-19, and Table 1-20, respectively.

Table 1-18: **VITA 57.1 FMC1 HPC Connections at J112**

FPGA Pin	Net Name	FMC Pin
D11	FMC1_CLK0_M2C_P	H4
E11	FMC1_CLK0_M2C_N	H5
V30	FMC1_CLK1_M2C_P	G2
W30	FMC1_CLK1_M2C_N	G3
N33	FMC1_CLK2_M2C_P	K4
M33	FMC1_CLK2_M2C_N	K5
D34	FMC1_CLK3_M2C_P	J2
C34	FMC1_CLK3_M2C_N	J3
AG27	FMC1_HA00_CC_P	F4
AG28	FMC1_HA00_CC_N	F5
AN33	FMC1_HA01_CC_P	E2
AN34	FMC1_HA01_CC_N	E3
AD25	FMC1_HA02_P	K7
AD26	FMC1_HA02_N	K8
AE27	FMC1_HA03_P	J6

Table 1-18: **VITA 57.1 FMC1 HPC Connections at J112 *(Cont'd)***

FPGA Pin	Net Name	FMC Pin
AD27	FMC1_HA03_N	J7
AH33	FMC1_HA04_P	F7
AH32	FMC1_HA04_N	F8
AE28	FMC1_HA05_P	E6
AE29	FMC1_HA05_N	E7
AJ34	FMC1_HA06_P	K10
AH34	FMC1_HA06_N	K11
AF28	FMC1_HA07_P	J9
AF29	FMC1_HA07_N	J10
AL34	FMC1_HA08_P	F10
AK34	FMC1_HA08_N	F11
AH29	FMC1_HA09_P	E9
AH30	FMC1_HA09_N	E10
AF26	FMC1_HA10_P	K13
AE26	FMC1_HA10_N	K14
AJ31	FMC1_HA11_P	J12
AJ32	FMC1_HA11_N	J13
AJ29	FMC1_HA12_P	F13
AJ30	FMC1_HA12_N	F14
AK33	FMC1_HA13_P	E12
AK32	FMC1_HA13_N	E13
AL31	FMC1_HA14_P	J15
AK31	FMC1_HA14_N	J16
AM33	FMC1_HA15_P	F16
AL33	FMC1_HA15_N	F17
AN32	FMC1_HA16_P	E15
AM32	FMC1_HA16_N	E16
AF30	FMC1_HA17_CC_P	K16
AG30	FMC1_HA17_CC_N	K17
AP32	FMC1_HA18_P	J18
AP33	FMC1_HA18_N	J19
AL30	FMC1_HA19_P	F19
AM31	FMC1_HA19_N	F20

Table 1-18: **VITA 57.1 FMC1 HPC Connections at J112 *(Cont'd)***

FPGA Pin	Net Name	FMC Pin
AB25	FMC1_HA20_P	E18
AC25	FMC1_HA20_N	E19
AA30	FMC1_HA21_P	K19
AA31	FMC1_HA21_N	K20
AA34	FMC1_HA22_P	J21
AA33	FMC1_HA22_N	J22
N28	FMC1_HB00_CC_P	K25
N29	FMC1_HB00_CC_N	K26
M31	FMC1_HB01_P	J24
L31	FMC1_HB01_N	J25
N25	FMC1_HB02_P	F22
M25	FMC1_HB02_N	F23
M26	FMC1_HB03_P	E21
M27	FMC1_HB03_N	E22
P31	FMC1_HB04_P	F25
P30	FMC1_HB04_N	F26
N27	FMC1_HB05_P	E24
P27	FMC1_HB05_N	E25
N32	FMC1_HB06_CC_P	K28
P32	FMC1_HB06_CC_N	K29
L33	FMC1_HB07_P	J27
M32	FMC1_HB07_N	J28
L28	FMC1_HB08_P	F28
M28	FMC1_HB08_N	F29
R28	FMC1_HB09_P	E27
R27	FMC1_HB09_N	E28
R31	FMC1_HB10_P	K31
R32	FMC1_HB10_N	K32
R26	FMC1_HB11_P	J30
T26	FMC1_HB11_N	J31
K34	FMC1_HB12_P	F31
L34	FMC1_HB12_N	F32
M30	FMC1_HB13_P	E30

Table 1-18: **VITA 57.1 FMC1 HPC Connections at J112 *(Cont'd)***

FPGA Pin	Net Name	FMC Pin
N30	FMC1_HB13_N	E31
N34	FMC1_HB14_P	K34
P34	FMC1_HB14_N	K35
P29	FMC1_HB15_P	J33
R29	FMC1_HB15_N	J34
L29	FMC1_HB16_P	F34
L30	FMC1_HB16_N	F35
F33	FMC1_HB17_CC_P	K37
G33	FMC1_HB17_CC_N	K38
C32	FMC1_HB18_P	J36
B32	FMC1_HB18_N	J37
J26	FMC1_HB19_P	E33
J27	FMC1_HB19_N	E34
L25	FMC1_HB20_P	F37
L26	FMC1_HB20_N	F38
J31	FMC1_HB21_P	E36
J32	FMC1_HB21_N	E37
U27.9	FMC1_I2C_SCL(1)	C30
U27.8	FMC1_I2C_SDA(1)	C31
AD30	FMC1_LA00_CC_P	G6
AC30	FMC1_LA00_CC_N	G7
AE34	FMC1_LA01_CC_P	D8
AF34	FMC1_LA01_CC_N	D9
AD34	FMC1_LA02_P	H7
AC34	FMC1_LA02_N	H8
AB30	FMC1_LA03_P	G9
AB31	FMC1_LA03_N	G10
AC33	FMC1_LA04_P	H10
AB33	FMC1_LA04_N	H11
AE31	FMC1_LA05_P	D11
AD31	FMC1_LA05_N	D12
AA25	FMC1_LA06_P	C10
Y26	FMC1_LA06_N	C11

Table 1-18: **VITA 57.1 FMC1 HPC Connections at J112 *(Cont'd)***

FPGA Pin	Net Name	FMC Pin
AA28	FMC1_LA07_P	H13
AA29	FMC1_LA07_N	H14
AE33	FMC1_LA08_P	G12
AF33	FMC1_LA08_N	G13
AD29	FMC1_LA09_P	D14
AC29	FMC1_LA09_N	D15
AB32	FMC1_LA10_P	C14
AC32	FMC1_LA10_N	C15
AB28	FMC1_LA11_P	H16
AC28	FMC1_LA11_N	H17
AD32	FMC1_LA12_P	G15
AE32	FMC1_LA12_N	G16
AB27	FMC1_LA13_P	D17
AC27	FMC1_LA13_N	D18
AG33	FMC1_LA14_P	C18
AG32	FMC1_LA14_N	C19
AA26	FMC1_LA15_P	H19
AB26	FMC1_LA15_N	H20
AG31	FMC1_LA16_P	G18
AF31	FMC1_LA16_N	G19
V34	FMC1_LA17_CC_P	D20
W34	FMC1_LA17_CC_N	D21
V28	FMC1_LA18_CC_P	C22
V27	FMC1_LA18_CC_N	C23
U25	FMC1_LA19_P	H22
T25	FMC1_LA19_N	H23
T28	FMC1_LA20_P	G21
T29	FMC1_LA20_N	G22
R33	FMC1_LA21_P	H25
R34	FMC1_LA21_N	H26
T31	FMC1_LA22_P	G25
T30	FMC1_LA22_N	G24
T34	FMC1_LA23_P	D24

Table 1-18: **VITA 57.1 FMC1 HPC Connections at J112 *(Cont'd)***

FPGA Pin	Net Name	FMC Pin
T33	FMC1_LA23_N	D23
U27	FMC1_LA24_P	H29
U26	FMC1_LA24_N	H28
U32	FMC1_LA25_P	G28
U33	FMC1_LA25_N	G27
V33	FMC1_LA26_P	D27
V32	FMC1_LA26_N	D26
Y31	FMC1_LA27_P	C27
Y32	FMC1_LA27_N	C26
Y34	FMC1_LA28_P	H32
Y33	FMC1_LA28_N	H31
Y29	FMC1_LA29_P	G31
W29	FMC1_LA29_N	G30
W32	FMC1_LA30_P	H35
W31	FMC1_LA30_N	H34
Y27	FMC1_LA31_P	G34
Y28	FMC1_LA31_N	G33
V25	FMC1_LA32_P	H38
W25	FMC1_LA32_N	H37
W26	FMC1_LA33_P	G37
W27	FMC1_LA33_N	G36
E34	FMC1_PRSNT_M2C_L	H2
U20.14	FMC1_TCK_BUF(1)	D29
J36.1	FMC1_TDI(1)	D30
J36.3	FMC1_TDO(1)	D31
U20.16	TMS_BUF(1)	D33

Notes:

1. This signal is not directly connected to the FPGA. The value in the leftmost column represents the device and pin the signal is connected to. For example, U27.9 = U27 pin 9.

Table 1-19: **VITA 57.1 FMC2 HPC Connections at J113**

FPGA Pin	Net Name	FMC Pin
K13	FMC2_CLK0_M2C_P	H4
K12	FMC2_CLK0_M2C_N	H5
J25	FMC2_CLK1_M2C_P	G2
J24	FMC2_CLK1_M2C_N	G3
C29	FMC2_CLK2_M2C_P	K4
D29	FMC2_CLK2_M2C_N	K5
F19	FMC2_CLK3_M2C_P	J2
F20	FMC2_CLK3_M2C_N	J3
AP20	FMC2_HA00_CC_P	F4
AP21	FMC2_HA00_CC_N	F5
AF19	FMC2_HA01_CC_P	E2
AE19	FMC2_HA01_CC_N	E3
AE21	FMC2_HA02_P	K7
AD21	FMC2_HA02_N	K8
AM18	FMC2_HA03_P	J6
AL18	FMC2_HA03_N	J7
AG22	FMC2_HA04_P	F7
AH22	FMC2_HA04_N	F8
AP19	FMC2_HA05_P	E6
AN18	FMC2_HA05_N	E7
AK22	FMC2_HA06_P	K10
AJ22	FMC2_HA06_N	K11
AN19	FMC2_HA07_P	J9
AN20	FMC2_HA07_N	J10
AC20	FMC2_HA08_P	F10
AD20	FMC2_HA08_N	F11
AM20	FMC2_HA09_P	E9
AL20	FMC2_HA09_N	E10
AF20	FMC2_HA10_P	K13
AF21	FMC2_HA10_N	K14
AJ20	FMC2_HA11_P	J12
AH20	FMC2_HA11_N	J13
AM21	FMC2_HA12_P	F13

Table 1-19: **VITA 57.1 FMC2 HPC Connections at J113 *(Cont'd)***

FPGA Pin	Net Name	FMC Pin
AL21	FMC2_HA12_N	F14
AC19	FMC2_HA13_P	E12
AD19	FMC2_HA13_N	E13
AM23	FMC2_HA14_P	J15
AL23	FMC2_HA14_N	J16
AK21	FMC2_HA15_P	F16
AJ21	FMC2_HA15_N	F17
AM22	FMC2_HA16_P	E15
AN22	FMC2_HA16_N	E16
AK19	FMC2_HA17_CC_P	K16
AL19	FMC2_HA17_CC_N	K17
AG20	FMC2_HA18_P	J18
AG21	FMC2_HA18_N	J19
AP22	FMC2_HA19_P	F19
AN23	FMC2_HA19_N	F20
AP25	FMC2_HA20_P	E18
AP24	FMC2_HA20_N	E19
AN30	FMC2_HA21_P	K19
AM30	FMC2_HA21_N	K20
AH27	FMC2_HA22_P	J21
AH28	FMC2_HA22_N	J22
C28	FMC2_HB00_CC_P	K25
B28	FMC2_HB00_CC_N	K26
D25	FMC2_HB01_P	J24
D26	FMC2_HB01_N	J25
C24	FMC2_HB02_P	F22
C25	FMC2_HB02_N	F23
E26	FMC2_HB03_P	E21
F26	FMC2_HB03_N	E22
B25	FMC2_HB04_P	F25
A25	FMC2_HB04_N	F26
D27	FMC2_HB05_P	E24
E27	FMC2_HB05_N	E25

Table 1-19: **VITA 57.1 FMC2 HPC Connections at J113 *(Cont'd)***

FPGA Pin	Net Name	FMC Pin
D24	FMC2_HB06_CC_P	K28
E24	FMC2_HB06_CC_N	K29
B26	FMC2_HB07_P	J27
A26	FMC2_HB07_N	J28
G26	FMC2_HB08_P	F28
G27	FMC2_HB08_N	F29
B27	FMC2_HB09_P	E27
C27	FMC2_HB09_N	E28
H27	FMC2_HB10_P	K31
G28	FMC2_HB10_N	K32
A28	FMC2_HB11_P	J30
A29	FMC2_HB11_N	J31
F28	FMC2_HB12_P	F31
E28	FMC2_HB12_N	F32
A30	FMC2_HB13_P	E30
B30	FMC2_HB13_N	E31
E29	FMC2_HB14_P	K34
F29	FMC2_HB14_N	K35
C30	FMC2_HB15_P	J33
D30	FMC2_HB15_N	J34
F25	FMC2_HB16_P	F34
G25	FMC2_HB16_N	F35
F21	FMC2_HB17_CC_P	K37
G20	FMC2_HB17_CC_N	K38
C20	FMC2_HB18_P	J36
D20	FMC2_HB18_N	J37
A23	FMC2_HB19_P	E33
A24	FMC2_HB19_N	E34
L20	FMC2_HB20_P	F37
L21	FMC2_HB20_N	F38
C22	FMC2_HB21_P	E36
D22	FMC2_HB21_N	E37
U27.11	FMC2_I2C_SCL(1)	C30

Table 1-19: **VITA 57.1 FMC2 HPC Connections at J113 *(Cont'd)***

FPGA Pin	Net Name	FMC Pin
U27.10	FMC2_I2C_SDA(1)	C31
AN27	FMC2_LA00_CC_P	G6
AM27	FMC2_LA00_CC_N	G7
AH25	FMC2_LA01_CC_P	D8
AJ25	FMC2_LA01_CC_N	D9
AG25	FMC2_LA02_P	H7
AG26	FMC2_LA02_N	H8
AP30	FMC2_LA03_P	G9
AP31	FMC2_LA03_N	G10
AL29	FMC2_LA04_P	H10
AK29	FMC2_LA04_N	H11
AN29	FMC2_LA05_P	D11
AP29	FMC2_LA05_N	D12
AL28	FMC2_LA06_P	C10
AK28	FMC2_LA06_N	C11
AN28	FMC2_LA07_P	H13
AM28	FMC2_LA07_N	H14
AK27	FMC2_LA08_P	G12
AJ27	FMC2_LA08_N	G13
AH23	FMC2_LA09_P	D14
AH24	FMC2_LA09_N	D15
AK26	FMC2_LA10_P	C14
AJ26	FMC2_LA10_N	C15
AL26	FMC2_LA11_P	H16
AM26	FMC2_LA11_N	H17
AJ24	FMC2_LA12_P	G15
AK24	FMC2_LA12_N	G16
AP27	FMC2_LA13_P	D17
AP26	FMC2_LA13_N	D18
AM25	FMC2_LA14_P	C18
AL25	FMC2_LA14_N	C19
AN25	FMC2_LA15_P	H19
AN24	FMC2_LA15_N	H20

Table 1-19: **VITA 57.1 FMC2 HPC Connections at J113 *(Cont'd)***

FPGA Pin	Net Name	FMC Pin
AK23	FMC2_LA16_P	G18
AL24	FMC2_LA16_N	G19
U23	FMC2_LA17_CC_P	D20
V23	FMC2_LA17_CC_N	D21
AD24	FMC2_LA18_CC_P	C22
AE24	FMC2_LA18_CC_N	C23
M23	FMC2_LA19_P	H22
L24	FMC2_LA19_N	H23
F24	FMC2_LA20_P	G21
F23	FMC2_LA20_N	G22
N23	FMC2_LA21_P	H25
N24	FMC2_LA21_N	H26
H23	FMC2_LA22_P	G24
G23	FMC2_LA22_N	G25
R24	FMC2_LA23_P	D23
P24	FMC2_LA23_N	D24
H25	FMC2_LA24_P	H28
H24	FMC2_LA24_N	H29
T24	FMC2_LA25_P	G27
T23	FMC2_LA25_N	G28
V24	FMC2_LA26_P	D26
W24	FMC2_LA26_N	D27
AF25	FMC2_LA27_P	C26
AF24	FMC2_LA27_N	C27
Y24	FMC2_LA28_P	H31
AA24	FMC2_LA28_N	H32
AF23	FMC2_LA29_P	G30
AG23	FMC2_LA29_N	G31
AA23	FMC2_LA30_P	H34
AB23	FMC2_LA30_N	H35
AE23	FMC2_LA31_P	G33
AE22	FMC2_LA31_N	G34
AC23	FMC2_LA32_P	H37

Table 1-19: **VITA 57.1 FMC2 HPC Connections at J113 *(Cont'd)***

FPGA Pin	Net Name	FMC Pin
AC24	FMC2_LA32_N	H38
AC22	FMC2_LA33_P	G36
AD22	FMC2_LA33_N	G37
A21	FMC2_PRSNT_M2C_L	H2
U20.13	FMC2_TCK_BUF(1)	D29
J37.1	FMC2_TDI(1)	D30
J37.3	FMC2_TDO(1)	D31
U20.16	TMS_BUF(1)	D33

Notes:

1. This signal is not directly connected to the FPGA. The value in the leftmost column represents the device and pin the signal is connected to. For example: U27.11 = U27 pin 11.

Table 1-20: **VITA 57.1 FMC3 HPC Connections at J115**

FPGA Pin	Net Name	FMC Pin
A10	FMC3_CLK0_M2C_P	H4
B10	FMC3_CLK0_M2C_N	H5
L10	FMC3_CLK1_M2C_P	G2
M10	FMC3_CLK1_M2C_N	G3
K16	FMC3_CLK2_M2C_P	K4
L16	FMC3_CLK2_M2C_N	K5
G18	FMC3_CLK3_M2C_P	J2
H18	FMC3_CLK3_M2C_N	J3
AC15	FMC3_HA00_CC_P	F4
AD15	FMC3_HA00_CC_N	F5
AH17	FMC3_HA01_CC_P	E2
AG17	FMC3_HA01_CC_N	E3
AG15	FMC3_HA02_P	K7
AF15	FMC3_HA02_N	K8
AK14	FMC3_HA03_P	J6
AJ14	FMC3_HA03_N	J7
AJ15	FMC3_HA04_P	F7
AH15	FMC3_HA04_N	F8
AL15	FMC3_HA05_P	E6

Table 1-20: **VITA 57.1 FMC3 HPC Connections at J115 *(Cont'd)***

FPGA Pin	Net Name	FMC Pin
AL14	FMC3_HA05_N	E7
AG16	FMC3_HA06_P	K10
AF16	FMC3_HA06_N	K11
AN15	FMC3_HA07_P	J9
AM15	FMC3_HA07_N	J10
AJ17	FMC3_HA08_P	F10
AJ16	FMC3_HA08_N	F11
AP16	FMC3_HA09_P	E9
AP15	FMC3_HA09_N	E10
AC18	FMC3_HA10_P	K13
AC17	FMC3_HA10_N	K14
AH18	FMC3_HA11_P	J12
AG18	FMC3_HA11_N	J13
AN17	FMC3_HA12_P	F13
AP17	FMC3_HA12_N	F14
AJ19	FMC3_HA13_P	E12
AH19	FMC3_HA13_N	E13
AM17	FMC3_HA14_P	J15
AM16	FMC3_HA14_N	J16
AD17	FMC3_HA15_P	F16
AE17	FMC3_HA15_N	F17
AK18	FMC3_HA16_P	E15
AK17	FMC3_HA16_N	E16
AE16	FMC3_HA17_CC_P	K16
AD16	FMC3_HA17_CC_N	K17
AE18	FMC3_HA18_P	J18
AF18	FMC3_HA18_N	J19
AL16	FMC3_HA19_P	F19
AK16	FMC3_HA19_N	F20
AP14	FMC3_HA20_P	E18
AN14	FMC3_HA20_N	E19
AJ11	FMC3_HA21_P	K19
AK11	FMC3_HA21_N	K20

Table 1-20: **VITA 57.1 FMC3 HPC Connections at J115 *(Cont'd)***

FPGA Pin	Net Name	FMC Pin
AE13	FMC3_HA22_P	J21
AE12	FMC3_HA22_N	J22
L13	FMC3_HB00_CC_P	K25
M13	FMC3_HB00_CC_N	K26
G13	FMC3_HB01_P	J24
H14	FMC3_HB01_N	J25
D14	FMC3_HB02_P	F22
C14	FMC3_HB02_N	F23
A13	FMC3_HB03_P	E21
A14	FMC3_HB03_N	E22
G12	FMC3_HB04_P	F25
H13	FMC3_HB04_N	F26
F14	FMC3_HB05_P	E24
E14	FMC3_HB05_N	E25
K14	FMC3_HB06_CC_P	K28
J14	FMC3_HB06_CC_N	K29
H10	FMC3_HB07_P	J27
G10	FMC3_HB07_N	J28
B12	FMC3_HB08_P	F28
B13	FMC3_HB08_N	F29
C13	FMC3_HB09_P	E27
C12	FMC3_HB09_N	E28
H12	FMC3_HB10_P	K31
J12	FMC3_HB10_N	K32
A11	FMC3_HB11_P	J30
B11	FMC3_HB11_N	J31
J11	FMC3_HB12_P	F31
J10	FMC3_HB12_N	F32
E13	FMC3_HB13_P	E30
F13	FMC3_HB13_N	E31
K11	FMC3_HB14_P	K34
L11	FMC3_HB14_N	K35
D12	FMC3_HB15_P	J33

Table 1-20: **VITA 57.1 FMC3 HPC Connections at J115 *(Cont'd)***

FPGA Pin	Net Name	FMC Pin
E12	FMC3_HB15_N	J34
M12	FMC3_HB16_P	F34
M11	FMC3_HB16_N	F35
L15	FMC3_HB17_CC_P	K37
L14	FMC3_HB17_CC_N	K38
F18	FMC3_HB18_P	J36
E17	FMC3_HB18_N	J37
E18	FMC3_HB19_P	E33
D17	FMC3_HB19_N	E34
H15	FMC3_HB20_P	F37
J15	FMC3_HB20_N	F38
D15	FMC3_HB21_P	E36
C15	FMC3_HB21_N	E37
U27.14	FMC3_I2C_SCL(1)	C30
U27.13	FMC3_I2C_SDA(1)	C31
AC13	FMC3_LA00_CC_P	G6
AC12	FMC3_LA00_CC_N	G7
AJ10	FMC3_LA01_CC_P	D8
AH10	FMC3_LA01_CC_N	D9
AD14	FMC3_LA02_P	H7
AC14	FMC3_LA02_N	H8
AK12	FMC3_LA03_P	G9
AJ12	FMC3_LA03_N	G10
AF11	FMC3_LA04_P	H10
AE11	FMC3_LA04_N	H11
AM10	FMC3_LA05_P	D11
AL10	FMC3_LA05_N	D12
AG11	FMC3_LA06_P	C10
AG10	FMC3_LA06_N	C11
AL11	FMC3_LA07_P	H13
AM11	FMC3_LA07_N	H14
AD12	FMC3_LA08_P	G12
AD11	FMC3_LA08_N	G13

Table 1-20: **VITA 57.1 FMC3 HPC Connections at J115 *(Cont'd)***

FPGA Pin	Net Name	FMC Pin
AP11	FMC3_LA09_P	D14
AP12	FMC3_LA09_N	D15
AF13	FMC3_LA10_P	C14
AG13	FMC3_LA10_N	C15
AM12	FMC3_LA11_P	H16
AN12	FMC3_LA11_N	H17
AE14	FMC3_LA12_P	G15
AF14	FMC3_LA12_N	G16
AN13	FMC3_LA13_P	D17
AM13	FMC3_LA13_N	D18
AG12	FMC3_LA14_P	C18
AH12	FMC3_LA14_N	C19
AK13	FMC3_LA15_P	H19
AL13	FMC3_LA15_N	H20
AH13	FMC3_LA16_P	G18
AH14	FMC3_LA16_N	G19
AC10	FMC3_LA17_CC_P	D20
AB10	FMC3_LA17_CC_N	D21
AH9	FMC3_LA18_CC_P	C22
AJ9	FMC3_LA18_CC_N	C23
F9	FMC3_LA19_P	H22
F10	FMC3_LA19_N	H23
C10	FMC3_LA20_P	G21
D10	FMC3_LA20_N	G22
C9	FMC3_LA21_P	H25
D9	FMC3_LA21_N	H26
A9	FMC3_LA22_P	G24
A8	FMC3_LA22_N	G25
E8	FMC3_LA23_P	D23
E9	FMC3_LA23_N	D24
B8	FMC3_LA24_P	H28
C8	FMC3_LA24_N	H29
L9	FMC3_LA25_P	G27

Table 1-20: **VITA 57.1 FMC3 HPC Connections at J115 *(Cont'd)***

FPGA Pin	Net Name	FMC Pin
K9	FMC3_LA25_N	G28
AD10	FMC3_LA26_P	D26
AC9	FMC3_LA26_N	D27
AK8	FMC3_LA27_P	C26
AL8	FMC3_LA27_N	C27
AD9	FMC3_LA28_P	H31
AE9	FMC3_LA28_N	H32
AK9	FMC3_LA29_P	G30
AL9	FMC3_LA29_N	G31
AF9	FMC3_LA30_P	H34
AF10	FMC3_LA30_N	H35
AN9	FMC3_LA31_P	G33
AP9	FMC3_LA31_N	G34
AG8	FMC3_LA32_P	H37
AH8	FMC3_LA32_N	H38
AN10	FMC3_LA33_P	G36
AP10	FMC3_LA33_N	G37
H17	FMC3_PRSNT_M2C_L	H2
U20.12	FMC3_TCK_BUF(1)	D29
J38.1	FMC3_TDI(1)	D30
J38.3	FMC3_TDO(1)	D31
U20.16	TMS_BUF(1)	D33

Notes:

1. This signal is not directly connected to the FPGA. The value in the leftmost column represents the device and pin the signal is connected to. For example: U27.14 = U27 pin 14.

Table 1-21: **Power Supply Voltages for the HPC Connector**

Voltage Supply	Allowable Voltage Range	Number of Pins	Maximum Amps	Tolerance	Maximum Capacitive Load
V_{ADJ}	Fixed 2.5V	4	4	±5%	1,000 µF
$3P3V_{AUX}$	3.3V	1	0.020	±5%	150 µF
3P3V	3.3V	4	3	±5%	1,000 µF
12P0V	12V	2	1	±5%	1,000 µF

System Monitor

[Figure 1-2, callout 22]

To view System Monitor measurements using the ChipScope™ Pro tool, place a jumper across pins 1–2 on headers J180, J181, and J182 of the System Monitor interface.

I²C Bus Management

[Figure 1-2, callout 23]

The I²C bus is controlled through U27, an 8-channel I²C-bus multiplexer (NXP Semiconductor PCA9547). The FPGA communicates with the multiplexer through I²C data and clock signals mapped to FPGA pins H34 and H33, respectively. The I²C idcode for the PCA9547 device is 0x70. The bus hosts five components:

- SuperClock-2 module
- GTX transceiver power supply module
- FMC1
- FMC2
- FMC3

An I²C component can be accessed by selecting the appropriate channel through the control register of the MUX as shown in Table 1-22.

Table 1-22: **I²C Channel Assignments**

U27 Channel	I²C Component
0	SuperClock-2 module
1	GTX transceiver power supply module
2	FMC1
3	FMC2
4	FMC3

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Appendix A

Default Jumper Positions

Table A-1 shows the 27 standard (black) shunts that must be installed on the board for proper operation. There are an additional 5 (red) shorting plugs that must be installed to enable the output of on-board, digitally-controlled power (Table A-2). These jumpers must always be installed except where specifically noted in this user guide. Refer to PCB Assembly Drawing 0431511 for the default placement of all on-board jumpers and their respective connectors as they are located on the board.

Table A-1: **Standard Shunts**

Connector	Name	Shunt Position	Quantity	Pins (Jumper Label)
J14	TI PWR INH	Installed	1	1–2 (AFX MB)
J290	UCD9240 CTRL PIN	Installed	1	1–2 (ALWAYS ON)
J33	*VCC5 REG ENABLE*(1)	Installed Horizontally	2	1–2, 3–4
J19	VCC5 REG INH	Installed	1	1–2 (AFX)
J176	VFS VCCAUX ENABLE	Installed	1	1–2
J188	*SYSTEM CLOCK*(1)	Installed Horizontally	2	1–3, 2–4 (LVDS)
J292	PMBUS ALERT	Installed	1	2–3 (AFX)
J293	PMBUS CTRL	Installed	1	2–3 (AFX)
J294	PMBUS CLK	Installed	1	2–3 (AFX)
J295	PMBUS DATA	Installed	1	2–3 (AFX)
J24	*PMBUS LEVEL TRANSLATION*(1)	Installed	1	1–2 (AFX)
J119	*PMBUS LEVEL TRANSLATION*(1)	Installed	1	1–2 (VSMBUS)
J35	PWR MOD JTAG	Installed	1	2–3
J162	JTAG FMC BYPASS	Installed	1	1–2
J4	SYSTEM ACE CLOCK	Installed	1	1–2 (ON)
J22	SYSACE JTAG ENABLE	Installed	1	1–2
J23	SYSACE JTAG ENABLE	Installed	1	1–2
J195	SYSACE JTAG ENABLE	Installed	1	1–2
J196	SYSACE JTAG ENABLE	Installed	1	1–2
J180	AVDD_0	Installed	1	1–2 (ALT)
J181	ALT_AVDD	Installed	1	1–2 (AUX_FILT)

Table A-1: **Standard Shunts *(Cont'd)***

Connector	Name	Shunt Position	Quantity	Pins (Jumper Label)
J182	*VREF SELECT*(1)	Installed	1	1–2 (VREF)
J36	FMC1 JTAG	Installed	1	2–3
J37	FMC2 JTAG	Installed	1	2–3
J38	FMC3 JTAG	Installed	1	2–3

Notes:

1. Italicized entries in the Name column are not visible in the PCB silkscreen labels.

Table A-2: **Digital Power Shorting Plugs**

Connector	Name	Shorting Plug Position
J30	VCC3V3	Installed
J31	VCC2V5	Installed
J102	VCCINT	Installed
J104	VCCAUX	Installed
J105	VCCO	Installed

VITA 57.1 FMC HPC Connector Pinout

Table B-1 provides a cross-reference of signal names to pin coordinates for the VITA 57.1 FMC HPC connector.

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	RES1	GND
2	GND	CLK3_M2C_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_M2C_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_M2C_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_M2C_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND

UG724_aB_01_030410

Figure B-1: **FMC HPC Connector Pinout**

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Appendix C

ML623 Master UCF Listing

The ML623 master user constraints file (UCF) template provides for designs targeting the ML623 Virtex-6 FPGA GTX transceiver characterization board. Net names in the constraints listed below correlate with net names on the ML623 board schematic. Users must identify the appropriate pins and replace the net names below with net names in the user RTL. See the Constraints Guide for more information.

Users can refer to the UCF files generated by tools such as Memory Interface Generator (MIG) for memory interfaces and Base System Builder (BSB) for more detailed I/O standards information required for each particular interface. The FMC connectors J112, J113, and J115 are connected to 2.5V V_{cco} banks. Because each user's FMC card implements customer-specific circuitry, the FMC bank I/O standards must be uniquely defined by each customer.

ML623 Master UCF Listing:

```
NET "112_REFCLK0_N"          LOC = "AK5";
NET "112_REFCLK0_P"          LOC = "AK6";
NET "112_REFCLK1_N"          LOC = "AH5";
NET "112_REFCLK1_P"          LOC = "AH6";
NET "112_RX0_N"              LOC = "AP6";
NET "112_RX0_P"              LOC = "AP5";
NET "112_RX1_N"              LOC = "AM6";
NET "112_RX1_P"              LOC = "AM5";
NET "112_RX2_N"              LOC = "AL4";
NET "112_RX2_P"              LOC = "AL3";
NET "112_RX3_N"              LOC = "AJ4";
NET "112_RX3_P"              LOC = "AJ3";
NET "112_TX0_N"              LOC = "AP2";
NET "112_TX0_P"              LOC = "AP1";
NET "112_TX1_N"              LOC = "AN4";
NET "112_TX1_P"              LOC = "AN3";
NET "112_TX2_N"              LOC = "AM2";
NET "112_TX2_P"              LOC = "AM1";
NET "112_TX3_N"              LOC = "AK2";
NET "112_TX3_P"              LOC = "AK1";
NET "113_REFCLK0_N"          LOC = "AD5";
NET "113_REFCLK0_P"          LOC = "AD6";
NET "113_REFCLK1_N"          LOC = "AB5";
NET "113_REFCLK1_P"          LOC = "AB6";
NET "113_RX0_N"              LOC = "AG4";
NET "113_RX0_P"              LOC = "AG3";
NET "113_RX1_N"              LOC = "AF6";
NET "113_RX1_P"              LOC = "AF5";
NET "113_RX2_N"              LOC = "AE4";
NET "113_RX2_P"              LOC = "AE3";
NET "113_RX3_N"              LOC = "AC4";
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```
NET "113_RX3_P"             LOC = "AC3";
NET "113_TX0_N"             LOC = "AH2";
NET "113_TX0_P"             LOC = "AH1";
NET "113_TX1_N"             LOC = "AF2";
NET "113_TX1_P"             LOC = "AF1";
NET "113_TX2_N"             LOC = "AD2";
NET "113_TX2_P"             LOC = "AD1";
NET "113_TX3_N"             LOC = "AB2";
NET "113_TX3_P"             LOC = "AB1";
NET "114_REFCLK0_N"         LOC = "V5";
NET "114_REFCLK0_P"         LOC = "V6";
NET "114_REFCLK1_N"         LOC = "T5";
NET "114_REFCLK1_P"         LOC = "T6";
NET "114_RX0_N"             LOC = "AA4";
NET "114_RX0_P"             LOC = "AA3";
NET "114_RX1_N"             LOC = "W4";
NET "114_RX1_P"             LOC = "W3";
NET "114_RX2_N"             LOC = "U4";
NET "114_RX2_P"             LOC = "U3";
NET "114_RX3_N"             LOC = "R4";
NET "114_RX3_P"             LOC = "R3";
NET "114_TX0_N"             LOC = "Y2";
NET "114_TX0_P"             LOC = "Y1";
NET "114_TX1_N"             LOC = "V2";
NET "114_TX1_P"             LOC = "V1";
NET "114_TX2_N"             LOC = "T2";
NET "114_TX2_P"             LOC = "T1";
NET "114_TX3_N"             LOC = "P2";
NET "114_TX3_P"             LOC = "P1";
NET "115_REFCLK0_N"         LOC = "P5";
NET "115_REFCLK0_P"         LOC = "P6";
NET "115_REFCLK1_N"         LOC = "M5";
NET "115_REFCLK1_P"         LOC = "M6";
NET "115_RX0_N"             LOC = "N4";
NET "115_RX0_P"             LOC = "N3";
NET "115_RX1_N"             LOC = "L4";
NET "115_RX1_P"             LOC = "L3";
NET "115_RX2_N"             LOC = "K6";
NET "115_RX2_P"             LOC = "K5";
NET "115_RX3_N"             LOC = "J4";
NET "115_RX3_P"             LOC = "J3";
NET "115_TX0_N"             LOC = "M2";
NET "115_TX0_P"             LOC = "M1";
NET "115_TX1_N"             LOC = "K2";
NET "115_TX1_P"             LOC = "K1";
NET "115_TX2_N"             LOC = "H2";
NET "115_TX2_P"             LOC = "H1";
NET "115_TX3_N"             LOC = "F2";
NET "115_TX3_P"             LOC = "F1";
NET "116_REFCLK0_N"         LOC = "H5";
NET "116_REFCLK0_P"         LOC = "H6";
NET "116_REFCLK1_N"         LOC = "F5";
NET "116_REFCLK1_P"         LOC = "F6";
NET "116_RX0_N"             LOC = "G4";
NET "116_RX0_P"             LOC = "G3";
NET "116_RX1_N"             LOC = "E4";
NET "116_RX1_P"             LOC = "E3";
NET "116_RX2_N"             LOC = "D6";
NET "116_RX2_P"             LOC = "D5";
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NET "116_RX3_N"             LOC = "B6";
NET "116_RX3_P"             LOC = "B5";
NET "116_TX0_N"             LOC = "D2";
NET "116_TX0_P"             LOC = "D1";
NET "116_TX1_N"             LOC = "C4";
NET "116_TX1_P"             LOC = "C3";
NET "116_TX2_N"             LOC = "B2";
NET "116_TX2_P"             LOC = "B1";
NET "116_TX3_N"             LOC = "A4";
NET "116_TX3_P"             LOC = "A3";
NET "CCLK_0"                LOC = "K8";
NET "CLK_A"                 LOC = "H28";
NET "CLK_B"                 LOC = "K24";
NET "CLK_DIFF_A_N"          LOC = "A31";
NET "CLK_DIFF_A_P"          LOC = "B31";
NET "CLK_DIFF_B_N"          LOC = "M22";
NET "CLK_DIFF_B_P"          LOC = "L23";
NET "CM_CTRL_0"             LOC = "C18";
NET "CM_CTRL_1"             LOC = "B18";
NET "CM_CTRL_10"            LOC = "E21";
NET "CM_CTRL_11"            LOC = "D21";
NET "CM_CTRL_12"            LOC = "H20";
NET "CM_CTRL_13"            LOC = "H19";
NET "CM_CTRL_14"            LOC = "A20";
NET "CM_CTRL_15"            LOC = "E23";
NET "CM_CTRL_16"            LOC = "E22";
NET "CM_CTRL_17"            LOC = "B22";
NET "CM_CTRL_18"            LOC = "B21";
NET "CM_CTRL_19"            LOC = "J21";
NET "CM_CTRL_2"             LOC = "K22";
NET "CM_CTRL_20"            LOC = "J20";
NET "CM_CTRL_21"            LOC = "C23";
NET "CM_CTRL_22"            LOC = "B23";
NET "CM_CTRL_23"            LOC = "G22";
NET "CM_CTRL_3"             LOC = "K21";
NET "CM_CTRL_4"             LOC = "A19";
NET "CM_CTRL_5"             LOC = "A18";
NET "CM_CTRL_6"             LOC = "J22";
NET "CM_CTRL_7"             LOC = "H22";
NET "CM_CTRL_8"             LOC = "D19";
NET "CM_CTRL_9"             LOC = "E19";
NET "CM_GCLK_N"             LOC = "B16";
NET "CM_GCLK_P"             LOC = "A16";
NET "CM_LVDS1_N"            LOC = "J16";
NET "CM_LVDS1_P"            LOC = "J17";
NET "CM_LVDS2_N"            LOC = "K17";
NET "CM_LVDS2_P"            LOC = "K18";
NET "CM_LVDS3_N"            LOC = "D16";
NET "CM_LVDS3_P"            LOC = "E16";
NET "CM_RST"                LOC = "G21";
NET "CS_B_0"                LOC = "F8";
NET "D_IN_0"                LOC = "H8";
NET "D_OUT_BUSY_0"          LOC = "AA8";
NET "DUT_I2C_SCL"           LOC = "H33";
NET "DUT_I2C_SDA"           LOC = "H34";
NET "DUT_PMB_ALERT"         LOC = "J34";
NET "DUT_PMB_CLK"           LOC = "H32";
NET "DUT_PMB_CTRL"          LOC = "K33";
NET "DUT_PMB_DATA"          LOC = "G32";
```

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NET "DUT_SPI_CS"            LOC = "A33";
NET "DUT_SPI_D"             LOC = "G31";
NET "DUT_SPI_Q"             LOC = "B33";
NET "DUT_SPI_SCK"           LOC = "H30";
NET "FMC1_CLK0_M2C_N"       LOC = "E11";
NET "FMC1_CLK0_M2C_P"       LOC = "D11";
NET "FMC1_CLK1_M2C_N"       LOC = "W30";
NET "FMC1_CLK1_M2C_P"       LOC = "V30";
NET "FMC1_CLK2_M2C_N"       LOC = "M33";
NET "FMC1_CLK2_M2C_P"       LOC = "N33";
NET "FMC1_CLK3_M2C_N"       LOC = "C34";
NET "FMC1_CLK3_M2C_P"       LOC = "D34";
NET "FMC1_HA00_CC_N"        LOC = "AG28";
NET "FMC1_HA00_CC_P"        LOC = "AG27";
NET "FMC1_HA01_CC_N"        LOC = "AN34";
NET "FMC1_HA01_CC_P"        LOC = "AN33";
NET "FMC1_HA02_N"           LOC = "AD26";
NET "FMC1_HA02_P"           LOC = "AD25";
NET "FMC1_HA03_N"           LOC = "AD27";
NET "FMC1_HA03_P"           LOC = "AE27";
NET "FMC1_HA04_N"           LOC = "AH32";
NET "FMC1_HA04_P"           LOC = "AH33";
NET "FMC1_HA05_N"           LOC = "AE29";
NET "FMC1_HA05_P"           LOC = "AE28";
NET "FMC1_HA06_N"           LOC = "AH34";
NET "FMC1_HA06_P"           LOC = "AJ34";
NET "FMC1_HA07_N"           LOC = "AF29";
NET "FMC1_HA07_P"           LOC = "AF28";
NET "FMC1_HA08_N"           LOC = "AK34";
NET "FMC1_HA08_P"           LOC = "AL34";
NET "FMC1_HA09_N"           LOC = "AH30";
NET "FMC1_HA09_P"           LOC = "AH29";
NET "FMC1_HA10_N"           LOC = "AE26";
NET "FMC1_HA10_P"           LOC = "AF26";
NET "FMC1_HA11_N"           LOC = "AJ32";
NET "FMC1_HA11_P"           LOC = "AJ31";
NET "FMC1_HA12_N"           LOC = "AJ30";
NET "FMC1_HA12_P"           LOC = "AJ29";
NET "FMC1_HA13_N"           LOC = "AK32";
NET "FMC1_HA13_P"           LOC = "AK33";
NET "FMC1_HA14_N"           LOC = "AK31";
NET "FMC1_HA14_P"           LOC = "AL31";
NET "FMC1_HA15_N"           LOC = "AL33";
NET "FMC1_HA15_P"           LOC = "AM33";
NET "FMC1_HA16_N"           LOC = "AM32";
NET "FMC1_HA16_P"           LOC = "AN32";
NET "FMC1_HA17_CC_N"        LOC = "AG30";
NET "FMC1_HA17_CC_P"        LOC = "AF30";
NET "FMC1_HA18_N"           LOC = "AP33";
NET "FMC1_HA18_P"           LOC = "AP32";
NET "FMC1_HA19_N"           LOC = "AM31";
NET "FMC1_HA19_P"           LOC = "AL30";
NET "FMC1_HA20_N"           LOC = "AC25";
NET "FMC1_HA20_P"           LOC = "AB25";
NET "FMC1_HA21_N"           LOC = "AA31";
NET "FMC1_HA21_P"           LOC = "AA30";
NET "FMC1_HA22_N"           LOC = "AA33";
NET "FMC1_HA22_P"           LOC = "AA34";
NET "FMC1_HB00_CC_N"        LOC = "N29";
```

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NET "FMC1_HB00_CC_P"        LOC = "N28";
NET "FMC1_HB01_N"           LOC = "L31";
NET "FMC1_HB01_P"           LOC = "M31";
NET "FMC1_HB02_N"           LOC = "M25";
NET "FMC1_HB02_P"           LOC = "N25";
NET "FMC1_HB03_N"           LOC = "M27";
NET "FMC1_HB03_P"           LOC = "M26";
NET "FMC1_HB04_N"           LOC = "P30";
NET "FMC1_HB04_P"           LOC = "P31";
NET "FMC1_HB05_N"           LOC = "P27";
NET "FMC1_HB05_P"           LOC = "N27";
NET "FMC1_HB06_CC_N"        LOC = "P32";
NET "FMC1_HB06_CC_P"        LOC = "N32";
NET "FMC1_HB07_N"           LOC = "M32";
NET "FMC1_HB07_P"           LOC = "L33";
NET "FMC1_HB08_N"           LOC = "M28";
NET "FMC1_HB08_P"           LOC = "L28";
NET "FMC1_HB09_N"           LOC = "R27";
NET "FMC1_HB09_P"           LOC = "R28";
NET "FMC1_HB10_N"           LOC = "R32";
NET "FMC1_HB10_P"           LOC = "R31";
NET "FMC1_HB11_N"           LOC = "T26";
NET "FMC1_HB11_P"           LOC = "R26";
NET "FMC1_HB12_N"           LOC = "L34";
NET "FMC1_HB12_P"           LOC = "K34";
NET "FMC1_HB13_N"           LOC = "N30";
NET "FMC1_HB13_P"           LOC = "M30";
NET "FMC1_HB14_N"           LOC = "P34";
NET "FMC1_HB14_P"           LOC = "N34";
NET "FMC1_HB15_N"           LOC = "R29";
NET "FMC1_HB15_P"           LOC = "P29";
NET "FMC1_HB16_N"           LOC = "L30";
NET "FMC1_HB16_P"           LOC = "L29";
NET "FMC1_HB17_CC_N"        LOC = "G33";
NET "FMC1_HB17_CC_P"        LOC = "F33";
NET "FMC1_HB18_N"           LOC = "B32";
NET "FMC1_HB18_P"           LOC = "C32";
NET "FMC1_HB19_N"           LOC = "J27";
NET "FMC1_HB19_P"           LOC = "J26";
NET "FMC1_HB20_N"           LOC = "L26";
NET "FMC1_HB20_P"           LOC = "L25";
NET "FMC1_HB21_N"           LOC = "J32";
NET "FMC1_HB21_P"           LOC = "J31";
NET "FMC1_LA00_CC_N"        LOC = "AC30";
NET "FMC1_LA00_CC_P"        LOC = "AD30";
NET "FMC1_LA01_CC_N"        LOC = "AF34";
NET "FMC1_LA01_CC_P"        LOC = "AE34";
NET "FMC1_LA02_N"           LOC = "AC34";
NET "FMC1_LA02_P"           LOC = "AD34";
NET "FMC1_LA03_N"           LOC = "AB31";
NET "FMC1_LA03_P"           LOC = "AB30";
NET "FMC1_LA04_N"           LOC = "AB33";
NET "FMC1_LA04_P"           LOC = "AC33";
NET "FMC1_LA05_N"           LOC = "AD31";
NET "FMC1_LA05_P"           LOC = "AE31";
NET "FMC1_LA06_N"           LOC = "Y26";
NET "FMC1_LA06_P"           LOC = "AA25";
NET "FMC1_LA07_N"           LOC = "AA29";
NET "FMC1_LA07_P"           LOC = "AA28";
```

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NET "FMC1_LA08_N"           LOC = "AF33";
NET "FMC1_LA08_P"           LOC = "AE33";
NET "FMC1_LA09_N"           LOC = "AC29";
NET "FMC1_LA09_P"           LOC = "AD29";
NET "FMC1_LA10_N"           LOC = "AC32";
NET "FMC1_LA10_P"           LOC = "AB32";
NET "FMC1_LA11_N"           LOC = "AC28";
NET "FMC1_LA11_P"           LOC = "AB28";
NET "FMC1_LA12_N"           LOC = "AE32";
NET "FMC1_LA12_P"           LOC = "AD32";
NET "FMC1_LA13_N"           LOC = "AC27";
NET "FMC1_LA13_P"           LOC = "AB27";
NET "FMC1_LA14_N"           LOC = "AG32";
NET "FMC1_LA14_P"           LOC = "AG33";
NET "FMC1_LA15_N"           LOC = "AB26";
NET "FMC1_LA15_P"           LOC = "AA26";
NET "FMC1_LA16_N"           LOC = "AF31";
NET "FMC1_LA16_P"           LOC = "AG31";
NET "FMC1_LA17_CC_N"        LOC = "W34";
NET "FMC1_LA17_CC_P"        LOC = "V34";
NET "FMC1_LA18_CC_N"        LOC = "V27";
NET "FMC1_LA18_CC_P"        LOC = "V28";
NET "FMC1_LA19_N"           LOC = "T25";
NET "FMC1_LA19_P"           LOC = "U25";
NET "FMC1_LA20_N"           LOC = "T29";
NET "FMC1_LA20_P"           LOC = "T28";
NET "FMC1_LA21_N"           LOC = "R34";
NET "FMC1_LA21_P"           LOC = "R33";
NET "FMC1_LA22_N"           LOC = "T31";
NET "FMC1_LA22_P"           LOC = "T30";
NET "FMC1_LA23_N"           LOC = "T34";
NET "FMC1_LA23_P"           LOC = "T33";
NET "FMC1_LA24_N"           LOC = "U27";
NET "FMC1_LA24_P"           LOC = "U26";
NET "FMC1_LA25_N"           LOC = "U32";
NET "FMC1_LA25_P"           LOC = "U33";
NET "FMC1_LA26_N"           LOC = "V33";
NET "FMC1_LA26_P"           LOC = "V32";
NET "FMC1_LA27_N"           LOC = "Y31";
NET "FMC1_LA27_P"           LOC = "Y32";
NET "FMC1_LA28_N"           LOC = "Y34";
NET "FMC1_LA28_P"           LOC = "Y33";
NET "FMC1_LA29_N"           LOC = "Y29";
NET "FMC1_LA29_P"           LOC = "W29";
NET "FMC1_LA30_N"           LOC = "W32";
NET "FMC1_LA30_P"           LOC = "W31";
NET "FMC1_LA31_N"           LOC = "Y27";
NET "FMC1_LA31_P"           LOC = "Y28";
NET "FMC1_LA32_N"           LOC = "V25";
NET "FMC1_LA32_P"           LOC = "W25";
NET "FMC1_LA33_N"           LOC = "W26";
NET "FMC1_LA33_P"           LOC = "W27";
NET "FMC1_PRSNT_M2C_L"      LOC = "E34";
NET "FMC2_CLK0_M2C_N"       LOC = "K12";
NET "FMC2_CLK0_M2C_P"       LOC = "K13";
NET "FMC2_CLK1_M2C_N"       LOC = "J24";
NET "FMC2_CLK1_M2C_P"       LOC = "J25";
NET "FMC2_CLK2_M2C_N"       LOC = "D29";
NET "FMC2_CLK2_M2C_P"       LOC = "C29";
```

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NET "FMC2_CLK3_M2C_N"       LOC = "F20";
NET "FMC2_CLK3_M2C_P"       LOC = "F19";
NET "FMC2_HA00_CC_N"        LOC = "AP21";
NET "FMC2_HA00_CC_P"        LOC = "AP20";
NET "FMC2_HA01_CC_N"        LOC = "AE19";
NET "FMC2_HA01_CC_P"        LOC = "AF19";
NET "FMC2_HA02_N"           LOC = "AD21";
NET "FMC2_HA02_P"           LOC = "AE21";
NET "FMC2_HA03_N"           LOC = "AL18";
NET "FMC2_HA03_P"           LOC = "AM18";
NET "FMC2_HA04_N"           LOC = "AH22";
NET "FMC2_HA04_P"           LOC = "AG22";
NET "FMC2_HA05_N"           LOC = "AN18";
NET "FMC2_HA05_P"           LOC = "AP19";
NET "FMC2_HA06_N"           LOC = "AJ22";
NET "FMC2_HA06_P"           LOC = "AK22";
NET "FMC2_HA07_N"           LOC = "AN20";
NET "FMC2_HA07_P"           LOC = "AN19";
NET "FMC2_HA08_N"           LOC = "AD20";
NET "FMC2_HA08_P"           LOC = "AC20";
NET "FMC2_HA09_N"           LOC = "AL20";
NET "FMC2_HA09_P"           LOC = "AM20";
NET "FMC2_HA10_N"           LOC = "AF21";
NET "FMC2_HA10_P"           LOC = "AF20";
NET "FMC2_HA11_N"           LOC = "AH20";
NET "FMC2_HA11_P"           LOC = "AJ20";
NET "FMC2_HA12_N"           LOC = "AL21";
NET "FMC2_HA12_P"           LOC = "AM21";
NET "FMC2_HA13_N"           LOC = "AD19";
NET "FMC2_HA13_P"           LOC = "AC19";
NET "FMC2_HA14_N"           LOC = "AL23";
NET "FMC2_HA14_P"           LOC = "AM23";
NET "FMC2_HA15_N"           LOC = "AJ21";
NET "FMC2_HA15_P"           LOC = "AK21";
NET "FMC2_HA16_N"           LOC = "AN22";
NET "FMC2_HA16_P"           LOC = "AM22";
NET "FMC2_HA17_CC_N"        LOC = "AL19";
NET "FMC2_HA17_CC_P"        LOC = "AK19";
NET "FMC2_HA18_N"           LOC = "AG21";
NET "FMC2_HA18_P"           LOC = "AG20";
NET "FMC2_HA19_N"           LOC = "AN23";
NET "FMC2_HA19_P"           LOC = "AP22";
NET "FMC2_HA20_N"           LOC = "AP24";
NET "FMC2_HA20_P"           LOC = "AP25";
NET "FMC2_HA21_N"           LOC = "AM30";
NET "FMC2_HA21_P"           LOC = "AN30";
NET "FMC2_HA22_N"           LOC = "AH28";
NET "FMC2_HA22_P"           LOC = "AH27";
NET "FMC2_HB00_CC_N"        LOC = "B28";
NET "FMC2_HB00_CC_P"        LOC = "C28";
NET "FMC2_HB01_N"           LOC = "D26";
NET "FMC2_HB01_P"           LOC = "D25";
NET "FMC2_HB02_N"           LOC = "C25";
NET "FMC2_HB02_P"           LOC = "C24";
NET "FMC2_HB03_N"           LOC = "F26";
NET "FMC2_HB03_P"           LOC = "E26";
NET "FMC2_HB04_N"           LOC = "A25";
NET "FMC2_HB04_P"           LOC = "B25";
NET "FMC2_HB05_N"           LOC = "E27";
```

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NET "FMC2_HB05_P"           LOC = "D27";
NET "FMC2_HB06_CC_N"        LOC = "E24";
NET "FMC2_HB06_CC_P"        LOC = "D24";
NET "FMC2_HB07_N"           LOC = "A26";
NET "FMC2_HB07_P"           LOC = "B26";
NET "FMC2_HB08_N"           LOC = "G27";
NET "FMC2_HB08_P"           LOC = "G26";
NET "FMC2_HB09_N"           LOC = "C27";
NET "FMC2_HB09_P"           LOC = "B27";
NET "FMC2_HB10_N"           LOC = "G28";
NET "FMC2_HB10_P"           LOC = "H27";
NET "FMC2_HB11_N"           LOC = "A29";
NET "FMC2_HB11_P"           LOC = "A28";
NET "FMC2_HB12_N"           LOC = "E28";
NET "FMC2_HB12_P"           LOC = "F28";
NET "FMC2_HB13_N"           LOC = "B30";
NET "FMC2_HB13_P"           LOC = "A30";
NET "FMC2_HB14_N"           LOC = "F29";
NET "FMC2_HB14_P"           LOC = "E29";
NET "FMC2_HB15_N"           LOC = "D30";
NET "FMC2_HB15_P"           LOC = "C30";
NET "FMC2_HB16_N"           LOC = "G25";
NET "FMC2_HB16_P"           LOC = "F25";
NET "FMC2_HB17_CC_N"        LOC = "G20";
NET "FMC2_HB17_CC_P"        LOC = "F21";
NET "FMC2_HB18_N"           LOC = "D20";
NET "FMC2_HB18_P"           LOC = "C20";
NET "FMC2_HB19_N"           LOC = "A24";
NET "FMC2_HB19_P"           LOC = "A23";
NET "FMC2_HB20_N"           LOC = "L21";
NET "FMC2_HB20_P"           LOC = "L20";
NET "FMC2_HB21_N"           LOC = "D22";
NET "FMC2_HB21_P"           LOC = "C22";
NET "FMC2_LA00_CC_N"        LOC = "AM27";
NET "FMC2_LA00_CC_P"        LOC = "AN27";
NET "FMC2_LA01_CC_N"        LOC = "AJ25";
NET "FMC2_LA01_CC_P"        LOC = "AH25";
NET "FMC2_LA02_N"           LOC = "AG26";
NET "FMC2_LA02_P"           LOC = "AG25";
NET "FMC2_LA03_N"           LOC = "AP31";
NET "FMC2_LA03_P"           LOC = "AP30";
NET "FMC2_LA04_N"           LOC = "AK29";
NET "FMC2_LA04_P"           LOC = "AL29";
NET "FMC2_LA05_N"           LOC = "AP29";
NET "FMC2_LA05_P"           LOC = "AN29";
NET "FMC2_LA06_N"           LOC = "AK28";
NET "FMC2_LA06_P"           LOC = "AL28";
NET "FMC2_LA07_N"           LOC = "AM28";
NET "FMC2_LA07_P"           LOC = "AN28";
NET "FMC2_LA08_N"           LOC = "AJ27";
NET "FMC2_LA08_P"           LOC = "AK27";
NET "FMC2_LA09_N"           LOC = "AH24";
NET "FMC2_LA09_P"           LOC = "AH23";
NET "FMC2_LA10_N"           LOC = "AJ26";
NET "FMC2_LA10_P"           LOC = "AK26";
NET "FMC2_LA11_N"           LOC = "AM26";
NET "FMC2_LA11_P"           LOC = "AL26";
NET "FMC2_LA12_N"           LOC = "AK24";
NET "FMC2_LA12_P"           LOC = "AJ24";
```

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NET "FMC2_LA13_N"           LOC = "AP26";
NET "FMC2_LA13_P"           LOC = "AP27";
NET "FMC2_LA14_N"           LOC = "AL25";
NET "FMC2_LA14_P"           LOC = "AM25";
NET "FMC2_LA15_N"           LOC = "AN24";
NET "FMC2_LA15_P"           LOC = "AN25";
NET "FMC2_LA16_N"           LOC = "AL24";
NET "FMC2_LA16_P"           LOC = "AK23";
NET "FMC2_LA17_CC_N"        LOC = "V23";
NET "FMC2_LA17_CC_P"        LOC = "U23";
NET "FMC2_LA18_CC_N"        LOC = "AE24";
NET "FMC2_LA18_CC_P"        LOC = "AD24";
NET "FMC2_LA19_N"           LOC = "L24";
NET "FMC2_LA19_P"           LOC = "M23";
NET "FMC2_LA20_N"           LOC = "F23";
NET "FMC2_LA20_P"           LOC = "F24";
NET "FMC2_LA21_N"           LOC = "N24";
NET "FMC2_LA21_P"           LOC = "N23";
NET "FMC2_LA22_N"           LOC = "G23";
NET "FMC2_LA22_P"           LOC = "H23";
NET "FMC2_LA23_N"           LOC = "P24";
NET "FMC2_LA23_P"           LOC = "R24";
NET "FMC2_LA24_N"           LOC = "H24";
NET "FMC2_LA24_P"           LOC = "H25";
NET "FMC2_LA25_N"           LOC = "T23";
NET "FMC2_LA25_P"           LOC = "T24";
NET "FMC2_LA26_N"           LOC = "W24";
NET "FMC2_LA26_P"           LOC = "V24";
NET "FMC2_LA27_N"           LOC = "AF24";
NET "FMC2_LA27_P"           LOC = "AF25";
NET "FMC2_LA28_N"           LOC = "AA24";
NET "FMC2_LA28_P"           LOC = "Y24";
NET "FMC2_LA29_N"           LOC = "AG23";
NET "FMC2_LA29_P"           LOC = "AF23";
NET "FMC2_LA30_N"           LOC = "AB23";
NET "FMC2_LA30_P"           LOC = "AA23";
NET "FMC2_LA31_N"           LOC = "AE22";
NET "FMC2_LA31_P"           LOC = "AE23";
NET "FMC2_LA32_N"           LOC = "AC24";
NET "FMC2_LA32_P"           LOC = "AC23";
NET "FMC2_LA33_N"           LOC = "AD22";
NET "FMC2_LA33_P"           LOC = "AC22";
NET "FMC2_PRSNT_M2C_L"      LOC = "A21";
NET "FMC3_CLK0_M2C_N"       LOC = "B10";
NET "FMC3_CLK0_M2C_P"       LOC = "A10";
NET "FMC3_CLK1_M2C_N"       LOC = "M10";
NET "FMC3_CLK1_M2C_P"       LOC = "L10";
NET "FMC3_CLK2_M2C_N"       LOC = "L16";
NET "FMC3_CLK2_M2C_P"       LOC = "K16";
NET "FMC3_CLK3_M2C_N"       LOC = "H18";
NET "FMC3_CLK3_M2C_P"       LOC = "G18";
NET "FMC3_HA00_CC_N"        LOC = "AD15";
NET "FMC3_HA00_CC_P"        LOC = "AC15";
NET "FMC3_HA01_CC_N"        LOC = "AG17";
NET "FMC3_HA01_CC_P"        LOC = "AH17";
NET "FMC3_HA02_N"           LOC = "AF15";
NET "FMC3_HA02_P"           LOC = "AG15";
NET "FMC3_HA03_N"           LOC = "AJ14";
NET "FMC3_HA03_P"           LOC = "AK14";
```

```
NET "FMC3_HA04_N"           LOC = "AH15";
NET "FMC3_HA04_P"           LOC = "AJ15";
NET "FMC3_HA05_N"           LOC = "AL14";
NET "FMC3_HA05_P"           LOC = "AL15";
NET "FMC3_HA06_N"           LOC = "AF16";
NET "FMC3_HA06_P"           LOC = "AG16";
NET "FMC3_HA07_N"           LOC = "AM15";
NET "FMC3_HA07_P"           LOC = "AN15";
NET "FMC3_HA08_N"           LOC = "AJ16";
NET "FMC3_HA08_P"           LOC = "AJ17";
NET "FMC3_HA09_N"           LOC = "AP15";
NET "FMC3_HA09_P"           LOC = "AP16";
NET "FMC3_HA10_N"           LOC = "AC17";
NET "FMC3_HA10_P"           LOC = "AC18";
NET "FMC3_HA11_N"           LOC = "AG18";
NET "FMC3_HA11_P"           LOC = "AH18";
NET "FMC3_HA12_N"           LOC = "AP17";
NET "FMC3_HA12_P"           LOC = "AN17";
NET "FMC3_HA13_N"           LOC = "AH19";
NET "FMC3_HA13_P"           LOC = "AJ19";
NET "FMC3_HA14_N"           LOC = "AM16";
NET "FMC3_HA14_P"           LOC = "AM17";
NET "FMC3_HA15_N"           LOC = "AE17";
NET "FMC3_HA15_P"           LOC = "AD17";
NET "FMC3_HA16_N"           LOC = "AK17";
NET "FMC3_HA16_P"           LOC = "AK18";
NET "FMC3_HA17_CC_N"        LOC = "AD16";
NET "FMC3_HA17_CC_P"        LOC = "AE16";
NET "FMC3_HA18_N"           LOC = "AF18";
NET "FMC3_HA18_P"           LOC = "AE18";
NET "FMC3_HA19_N"           LOC = "AK16";
NET "FMC3_HA19_P"           LOC = "AL16";
NET "FMC3_HA20_N"           LOC = "AN14";
NET "FMC3_HA20_P"           LOC = "AP14";
NET "FMC3_HA21_N"           LOC = "AK11";
NET "FMC3_HA21_P"           LOC = "AJ11";
NET "FMC3_HA22_N"           LOC = "AE12";
NET "FMC3_HA22_P"           LOC = "AE13";
NET "FMC3_HB00_CC_N"        LOC = "M13";
NET "FMC3_HB00_CC_P"        LOC = "L13";
NET "FMC3_HB01_N"           LOC = "H14";
NET "FMC3_HB01_P"           LOC = "G13";
NET "FMC3_HB02_N"           LOC = "C14";
NET "FMC3_HB02_P"           LOC = "D14";
NET "FMC3_HB03_N"           LOC = "A14";
NET "FMC3_HB03_P"           LOC = "A13";
NET "FMC3_HB04_N"           LOC = "H13";
NET "FMC3_HB04_P"           LOC = "G12";
NET "FMC3_HB05_N"           LOC = "E14";
NET "FMC3_HB05_P"           LOC = "F14";
NET "FMC3_HB06_CC_N"        LOC = "J14";
NET "FMC3_HB06_CC_P"        LOC = "K14";
NET "FMC3_HB07_N"           LOC = "G10";
NET "FMC3_HB07_P"           LOC = "H10";
NET "FMC3_HB08_N"           LOC = "B13";
NET "FMC3_HB08_P"           LOC = "B12";
NET "FMC3_HB09_N"           LOC = "C12";
NET "FMC3_HB09_P"           LOC = "C13";
NET "FMC3_HB10_N"           LOC = "J12";
```

```
NET "FMC3_HB10_P"           LOC = "H12";
NET "FMC3_HB11_N"           LOC = "B11";
NET "FMC3_HB11_P"           LOC = "A11";
NET "FMC3_HB12_N"           LOC = "J10";
NET "FMC3_HB12_P"           LOC = "J11";
NET "FMC3_HB13_N"           LOC = "F13";
NET "FMC3_HB13_P"           LOC = "E13";
NET "FMC3_HB14_N"           LOC = "L11";
NET "FMC3_HB14_P"           LOC = "K11";
NET "FMC3_HB15_N"           LOC = "E12";
NET "FMC3_HB15_P"           LOC = "D12";
NET "FMC3_HB16_N"           LOC = "M11";
NET "FMC3_HB16_P"           LOC = "M12";
NET "FMC3_HB17_CC_N"        LOC = "L14";
NET "FMC3_HB17_CC_P"        LOC = "L15";
NET "FMC3_HB18_N"           LOC = "E17";
NET "FMC3_HB18_P"           LOC = "F18";
NET "FMC3_HB19_N"           LOC = "D17";
NET "FMC3_HB19_P"           LOC = "E18";
NET "FMC3_HB20_N"           LOC = "J15";
NET "FMC3_HB20_P"           LOC = "H15";
NET "FMC3_HB21_N"           LOC = "C15";
NET "FMC3_HB21_P"           LOC = "D15";
NET "FMC3_LA00_CC_N"        LOC = "AC12";
NET "FMC3_LA00_CC_P"        LOC = "AC13";
NET "FMC3_LA01_CC_N"        LOC = "AH10";
NET "FMC3_LA01_CC_P"        LOC = "AJ10";
NET "FMC3_LA02_N"           LOC = "AC14";
NET "FMC3_LA02_P"           LOC = "AD14";
NET "FMC3_LA03_N"           LOC = "AJ12";
NET "FMC3_LA03_P"           LOC = "AK12";
NET "FMC3_LA04_N"           LOC = "AE11";
NET "FMC3_LA04_P"           LOC = "AF11";
NET "FMC3_LA05_N"           LOC = "AL10";
NET "FMC3_LA05_P"           LOC = "AM10";
NET "FMC3_LA06_N"           LOC = "AG10";
NET "FMC3_LA06_P"           LOC = "AG11";
NET "FMC3_LA07_N"           LOC = "AM11";
NET "FMC3_LA07_P"           LOC = "AL11";
NET "FMC3_LA08_N"           LOC = "AD11";
NET "FMC3_LA08_P"           LOC = "AD12";
NET "FMC3_LA09_N"           LOC = "AP12";
NET "FMC3_LA09_P"           LOC = "AP11";
NET "FMC3_LA10_N"           LOC = "AG13";
NET "FMC3_LA10_P"           LOC = "AF13";
NET "FMC3_LA11_N"           LOC = "AN12";
NET "FMC3_LA11_P"           LOC = "AM12";
NET "FMC3_LA12_N"           LOC = "AF14";
NET "FMC3_LA12_P"           LOC = "AE14";
NET "FMC3_LA13_N"           LOC = "AM13";
NET "FMC3_LA13_P"           LOC = "AN13";
NET "FMC3_LA14_N"           LOC = "AH12";
NET "FMC3_LA14_P"           LOC = "AG12";
NET "FMC3_LA15_N"           LOC = "AL13";
NET "FMC3_LA15_P"           LOC = "AK13";
NET "FMC3_LA16_N"           LOC = "AH14";
NET "FMC3_LA16_P"           LOC = "AH13";
NET "FMC3_LA17_CC_N"        LOC = "AB10";
NET "FMC3_LA17_CC_P"        LOC = "AC10";
```

```
NET "FMC3_LA18_CC_N"        LOC = "AJ9";
NET "FMC3_LA18_CC_P"        LOC = "AH9";
NET "FMC3_LA19_N"           LOC = "F10";
NET "FMC3_LA19_P"           LOC = "F9";
NET "FMC3_LA20_N"           LOC = "D10";
NET "FMC3_LA20_P"           LOC = "C10";
NET "FMC3_LA21_N"           LOC = "D9";
NET "FMC3_LA21_P"           LOC = "C9";
NET "FMC3_LA22_N"           LOC = "A8";
NET "FMC3_LA22_P"           LOC = "A9";
NET "FMC3_LA23_N"           LOC = "E9";
NET "FMC3_LA23_P"           LOC = "E8";
NET "FMC3_LA24_N"           LOC = "C8";
NET "FMC3_LA24_P"           LOC = "B8";
NET "FMC3_LA25_N"           LOC = "K9";
NET "FMC3_LA25_P"           LOC = "L9";
NET "FMC3_LA26_N"           LOC = "AC9";
NET "FMC3_LA26_P"           LOC = "AD10";
NET "FMC3_LA27_N"           LOC = "AL8";
NET "FMC3_LA27_P"           LOC = "AK8";
NET "FMC3_LA28_N"           LOC = "AE9";
NET "FMC3_LA28_P"           LOC = "AD9";
NET "FMC3_LA29_N"           LOC = "AL9";
NET "FMC3_LA29_P"           LOC = "AK9";
NET "FMC3_LA30_N"           LOC = "AF10";
NET "FMC3_LA30_P"           LOC = "AF9";
NET "FMC3_LA31_N"           LOC = "AP9";
NET "FMC3_LA31_P"           LOC = "AN9";
NET "FMC3_LA32_N"           LOC = "AH8";
NET "FMC3_LA32_P"           LOC = "AG8";
NET "FMC3_LA33_N"           LOC = "AP10";
NET "FMC3_LA33_P"           LOC = "AN10";
NET "IO_L15N_16_D32"        LOC = "D32";
NET "IO_L15P_16_D31"        LOC = "D31";
NET "IO_L8N_SRCC_14_U30"    LOC = "U30";
NET "IO_L8P_SRCC_14_U31"    LOC = "U31";
NET "IO_L9N_MRCC_16_K27"    LOC = "K27";
NET "IO_L9P_MRCC_16_K26"    LOC = "K26";
NET "IO_LVDS_CLK_N"         LOC = "H9";
NET "IO_LVDS_CLK_P"         LOC = "J9";
NET "LED1"                  LOC = "M15";
NET "LED2"                  LOC = "M16";
NET "LED3"                  LOC = "F15";
NET "LED4"                  LOC = "G15";
NET "LED5"                  LOC = "B15";
NET "LED6"                  LOC = "A15";
NET "LED7"                  LOC = "G16";
NET "PB_SW1"                LOC = "E31";
NET "PB_SW2"                LOC = "F31";
NET "RDWR_B_0"              LOC = "G8";
NET "SW1"                   LOC = "M17";
NET "SW2"                   LOC = "M18";
NET "SW3"                   LOC = "J19";
NET "SW4"                   LOC = "K19";
NET "SW5"                   LOC = "B17";
NET "SW6"                   LOC = "C17";
NET "SW7"                   LOC = "L18";
NET "SW8"                   LOC = "L19";
NET "USB_CTS"               LOC = "E32";
```

```
NET "USB_GPIO0"             LOC = "J29";
NET "USB_GPIO1"             LOC = "K28";
NET "USB_GPIO2"             LOC = "B34";
NET "USB_GPIO3"             LOC = "C33";
NET "USB_RTS"               LOC = "E33";
NET "USB_RX"                LOC = "F30";
NET "USB_TX"                LOC = "G30";
```

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Appendix D

References

Additional information relevant to Virtex®-6 devices, the ML623 Virtex-6 FPGA GTX transceiver characterization board, and intellectual property is available in the documents listed here:

- DS150, *Virtex-6 Family Overview*
- DS152, *Virtex-6 FPGA Data Sheet: DC and Switching Characteristics*
- UG360, *Virtex-6 FPGA Configuration User Guide*
- UG361, *Virtex-6 FPGA SelectIO Resources User Guide*
- UG362, *Virtex-6 FPGA User Guide: Clocking Resources*
- UG364, *Virtex-6 FPGA Configurable Logic Block User Guide*
- UG365, *Virtex-6 FPGA Packaging and Pinout Specifications*
- UG366, *Virtex-6 FPGA GTX Transceivers User Guide*
- UG370, *Virtex-6 FPGA System Monitor User Guide*
- DS581, *XPS External Peripheral Controller (EPC) Data Sheet*
- DS606, *XPS IIC Bus Interface (v2.00a) Data Sheet*
- HW-CLK-101-SCLK2 SuperClock-2 Module User Guide

To find additional documentation, see the Xilinx website at:

http://www.xilinx.com/support/documentation/index.htm.