



# M74HCT164

## 8 BIT SIPO SHIFT REGISTER

- HIGH SPEED:  
 $t_{PD} = 24 \text{ ns (TYP.)}$  at  $V_{CC} = 4.5V$
- LOW POWER DISSIPATION:  
 $I_{CC} = 4\mu A(\text{MAX.})$  at  $T_A = 25^\circ C$
- COMPATIBLE WITH TTL OUTPUTS :  
 $V_{IH} = 2V (\text{MIN.})$   $V_{IL} = 0.8V (\text{MAX})$
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \cong t_{PHL}$
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 4mA (\text{MIN})$
- PIN AND FUNCTION COMPATIBLE WITH  
 74 SERIES 164



### ORDER CODES

PACKAGE	TUBE	T & R
DIP	M74HCT164B1R	
SOP	M74HCT164M1R	M74HCT164RM13TR
TSSOP		M74HCT164TTR

### DESCRIPTION

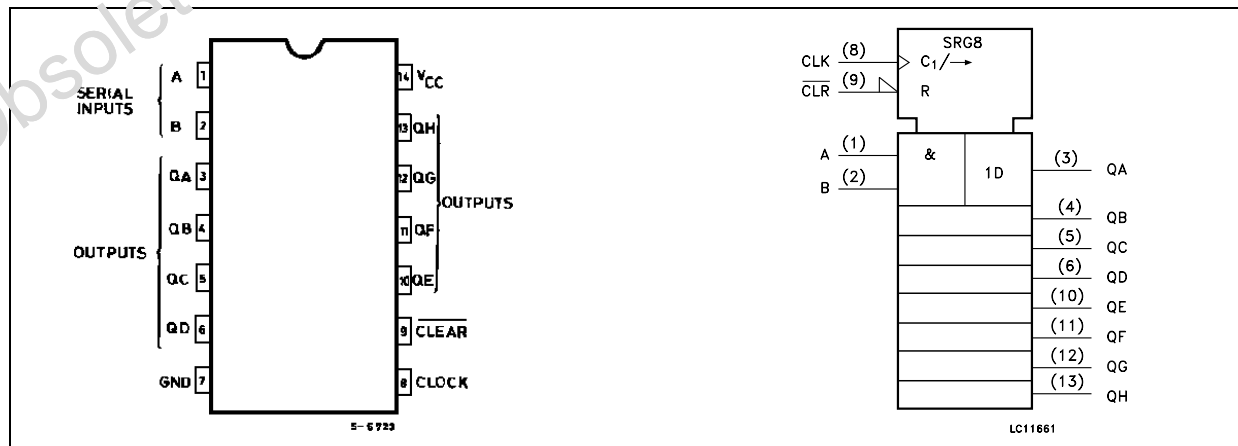
The M74HCT164 is an high speed CMOS 8 BIT SIPO SHIFT REGISTER fabricated with silicon gate C<sup>2</sup>MOS technology.

The 74HCT164 is an 8 bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B), either of these inputs can be used as an active high enable for data entry through the other input. An unused input must be high, or both inputs connected together. Each low-to-high transition on the clock inputs shifts data one place to the right and enters into QA, the logic NAND of

the two data inputs (A x B), the data that existed before the rising clock edge. A low level on the clear input overrides all other inputs and clears the register asynchronously, forcing all Q outputs low. The M74HCT164 is designed to directly interface HCMOS systems with TTL and NMOS components.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

### PIN CONNECTION AND IEC LOGIC SYMBOLS



# M74HCT164

## INPUT AND OUTPUT EQUIVALENT CIRCUIT



## PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1,2	A, B	Data Inputs
3, 4, 5, 6, 10, 11, 12, 13	QA to QH	Outputs
8	CLOCK	Clock Input (LOW to HIGH, Edge Triggered)
9	CLEAR	Master Reset Input
7	GND	Ground (0V)
14	Vcc	Positive Supply Voltage

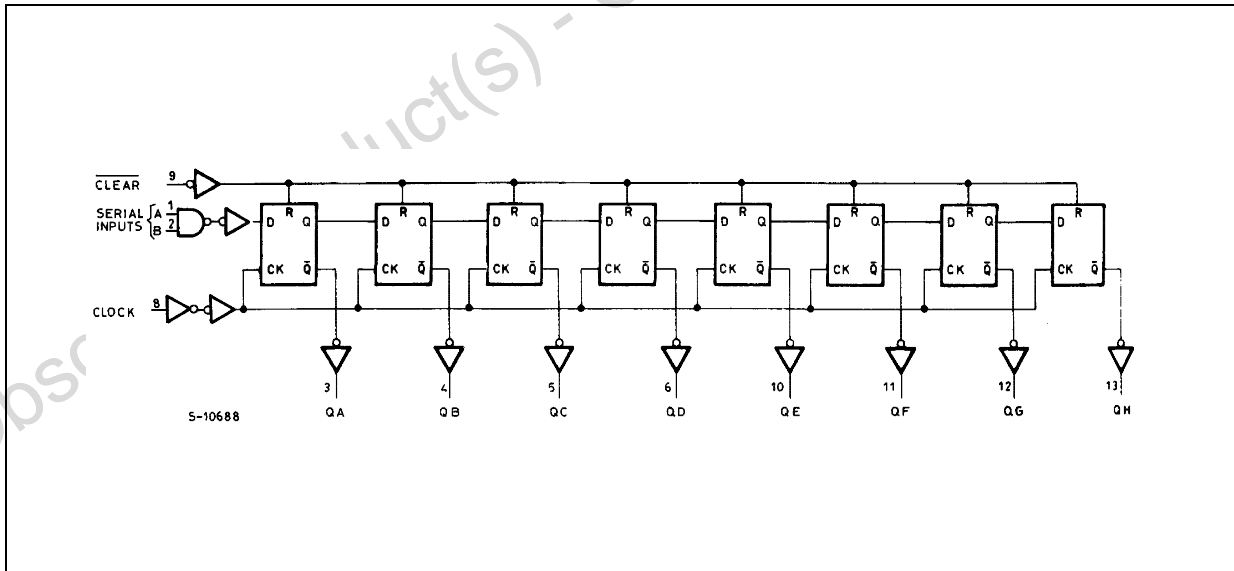
## TRUTH TABLE

INPUTS				OUTPUTS			
CLEAR	CLOCK	SERIAL IN		QA	QB	.....	QH
		A	B				
L	X	X	X	L	L	.....	L
H		X	X	NO CHANGE			
H		L	X	L	QAn	.....	QGn
H		X	L	L	QAn	.....	QGn
H		H	H	H	QAn	.....	QGn

X : Don't Care

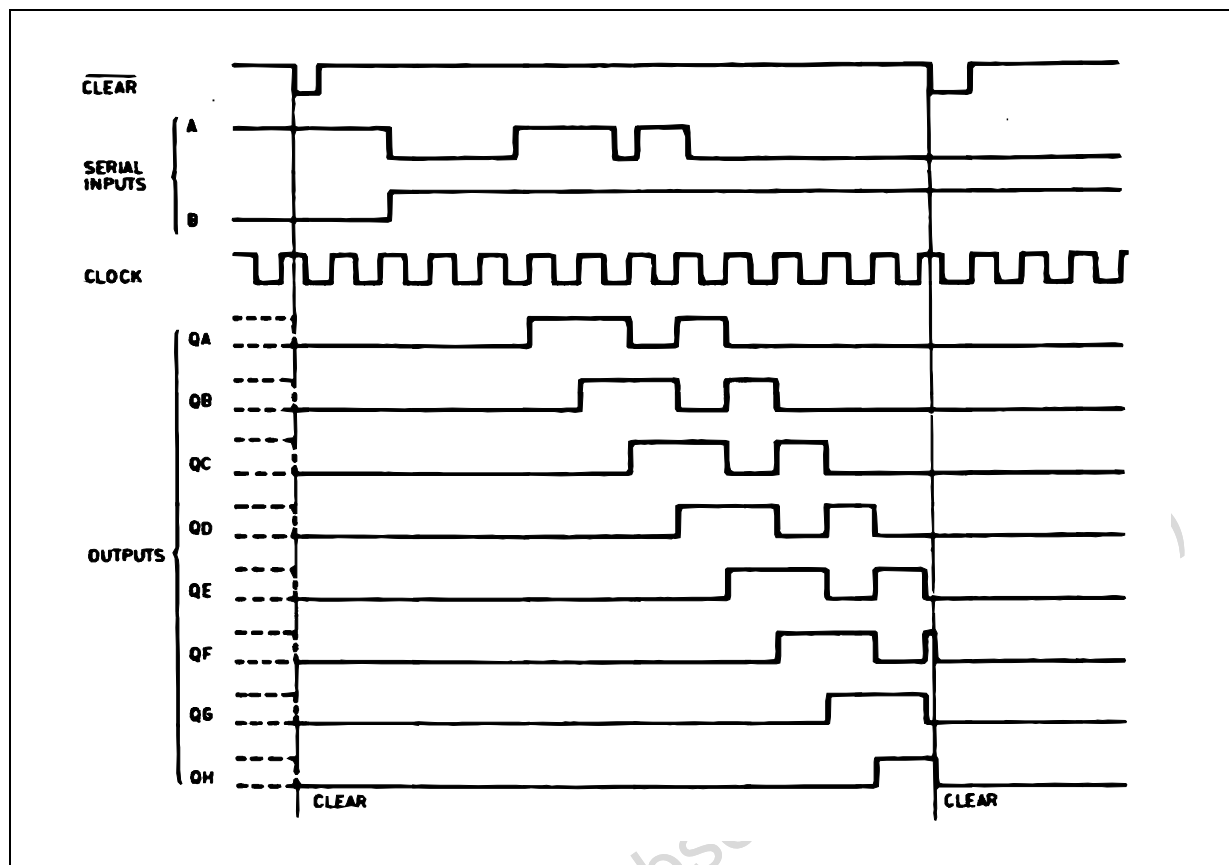
QAn - QGn : The level of QA - QG, respectively, before the most-recent transition of the clock

## LOGIC DIAGRAM



This logic diagram has not been used to estimate propagation delays

## TIMING CHART



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to +7	V
$V_I$	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
$V_O$	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	$\pm 20$	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Current	$\pm 25$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 50$	mA
$P_D$	Power Dissipation	500(*)	mW
$T_{stg}$	Storage Temperature	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (10 sec)	300	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

(\*) 500mW at 65  $^{\circ}C$ ; derate to 300mW by 10mW/ $^{\circ}C$  from 65 $^{\circ}C$  to 85 $^{\circ}C$

## M74HCT164

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	4.5 to 5.5	V
$V_I$	Input Voltage	0 to $V_{CC}$	V
$V_O$	Output Voltage	0 to $V_{CC}$	V
$T_{op}$	Operating Temperature	-55 to 125	°C
$t_r, t_f$	Input Rise and Fall Time ( $V_{CC} = 4.5$ to $5.5V$ )	0 to 500	ns

### DC SPECIFICATIONS

Symbol	Parameter	$V_{CC}$ (V)	Test Condition	Value						Unit	
				$T_A = 25^\circ C$			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$V_{IH}$	High Level Input Voltage	4.5 to 5.5		2.0			2.0		2.0		V
$V_{IL}$	Low Level Input Voltage	4.5 to 5.5				0.8		0.8		0.8	V
$V_{OH}$	High Level Output Voltage	4.5	$I_O = -20 \mu A$	4.4	4.5		4.4		4.4		V
			$I_O = -4.0 mA$	4.18	4.31		4.13		4.10		V
$V_{OL}$	Low Level Output Voltage	4.5	$I_O = 20 \mu A$		0.0	0.1		0.1		0.1	V
			$I_O = 4.0 mA$		0.17	0.26		0.33		0.40	V
$I_I$	Input Leakage Current	5.5	$V_I = V_{CC}$ or GND			$\pm 0.1$		$\pm 1$		$\pm 1$	$\mu A$
$I_{CC}$	Quiescent Supply Current	5.5	$V_I = V_{CC}$ or GND			4		40		80	$\mu A$
$\Delta I_{CC}$	Additional Worst Case Supply Current	5.5	Per Input pin $V_I = 0.5V$ or $V_I = 2.4V$ Other Inputs at $V_{CC}$ or GND $I_O = 0$			2.0		2.9		3.0	mA

AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$  pF, Input  $t_r = t_f = 6$  ns)

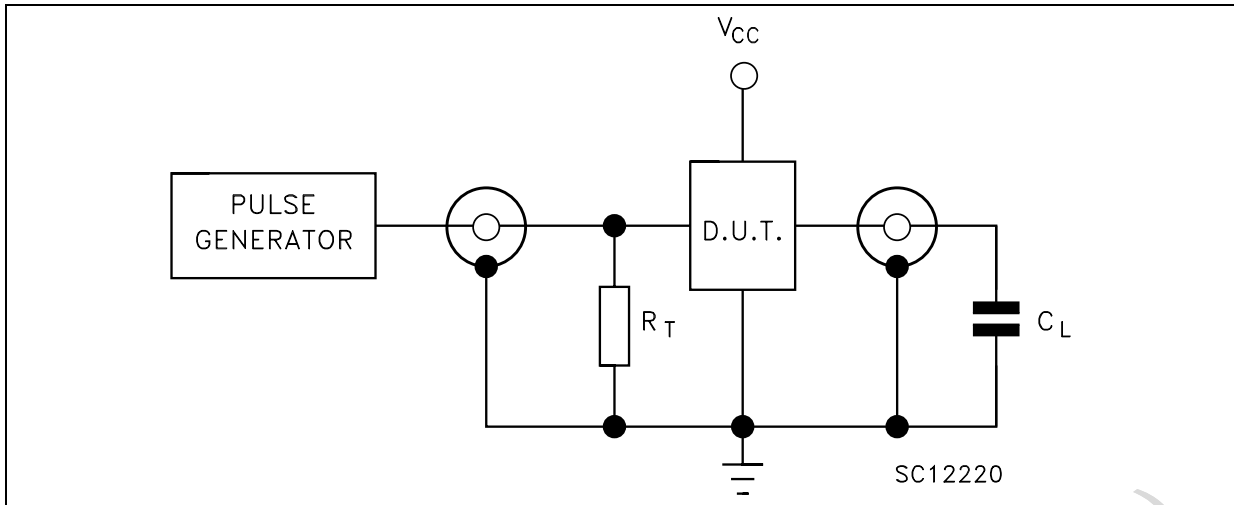
Symbol	Parameter	Test Condition		Value						Unit	
		$V_{CC}$ (V)		$T_A = 25^\circ\text{C}$			$-40$ to $85^\circ\text{C}$		$-55$ to $125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$t_{TLH}$ $t_{THL}$	Output Transition Time	4.5			8	15		19		22	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time (CLOCK - Q)	4.5			23	36		45		54	ns
$t_{PHL}$	Propagation Delay Time (CLEAR - Q)	4.5			24	37		46		56	ns
$f_{MAX}$	Maximum Clock Frequency	4.5		30	50		24		20		MHz
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	4.5			8	15		19		22	ns
$t_{W(L)}$	Minimum Pulse Width (CLEAR)	4.5			8	15		19		22	ns
$t_s$	Minimum Set-Up Time (A, B - CK)	4.5			4	10		13		15	ns
$t_h$	Minimum Hold Time (A, B - CK)	4.5				0		0		0	ns
$t_{REM}$	Minimum Removal Time	4.5				5		6		8	ns

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
		$V_{CC}$ (V)		$T_A = 25^\circ\text{C}$			$-40$ to $85^\circ\text{C}$		$-55$ to $125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$C_{IN}$	Input Capacitance				5	10		10		10	pF
$C_{PD}$	Power Dissipation Capacitance (note 1)				137						pF

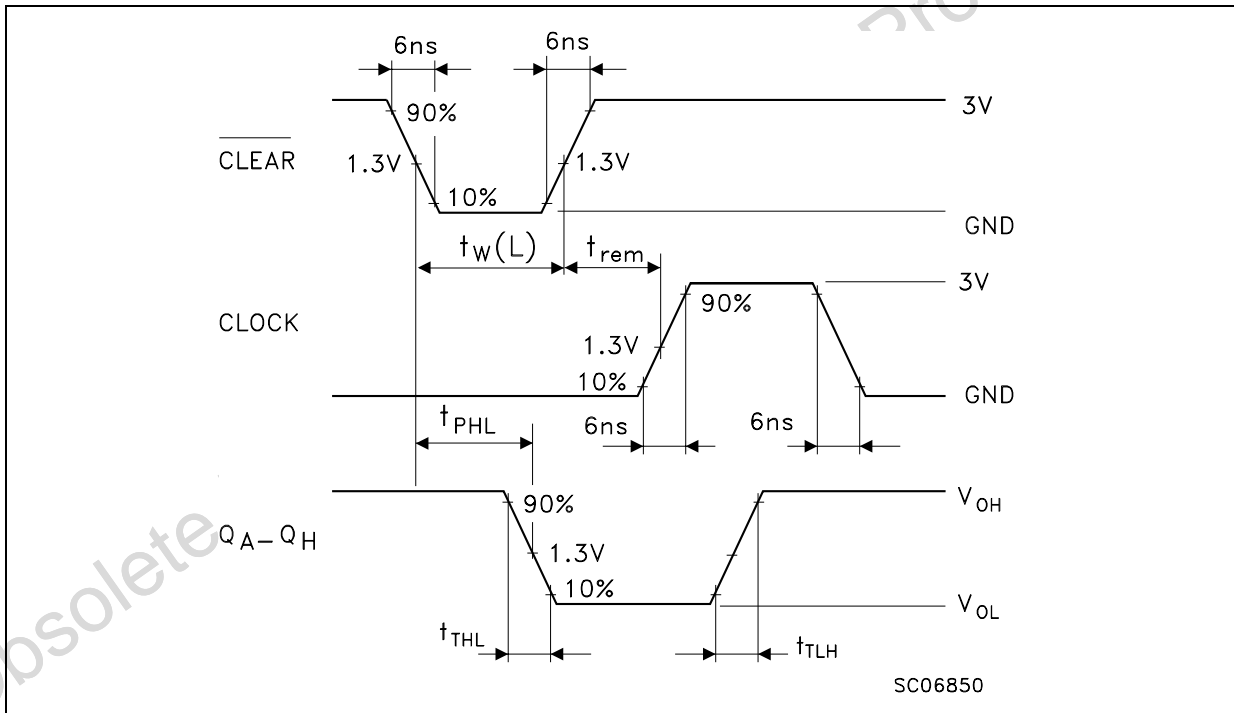
1)  $C_{PD}$  is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC(oper)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

TEST CIRCUIT

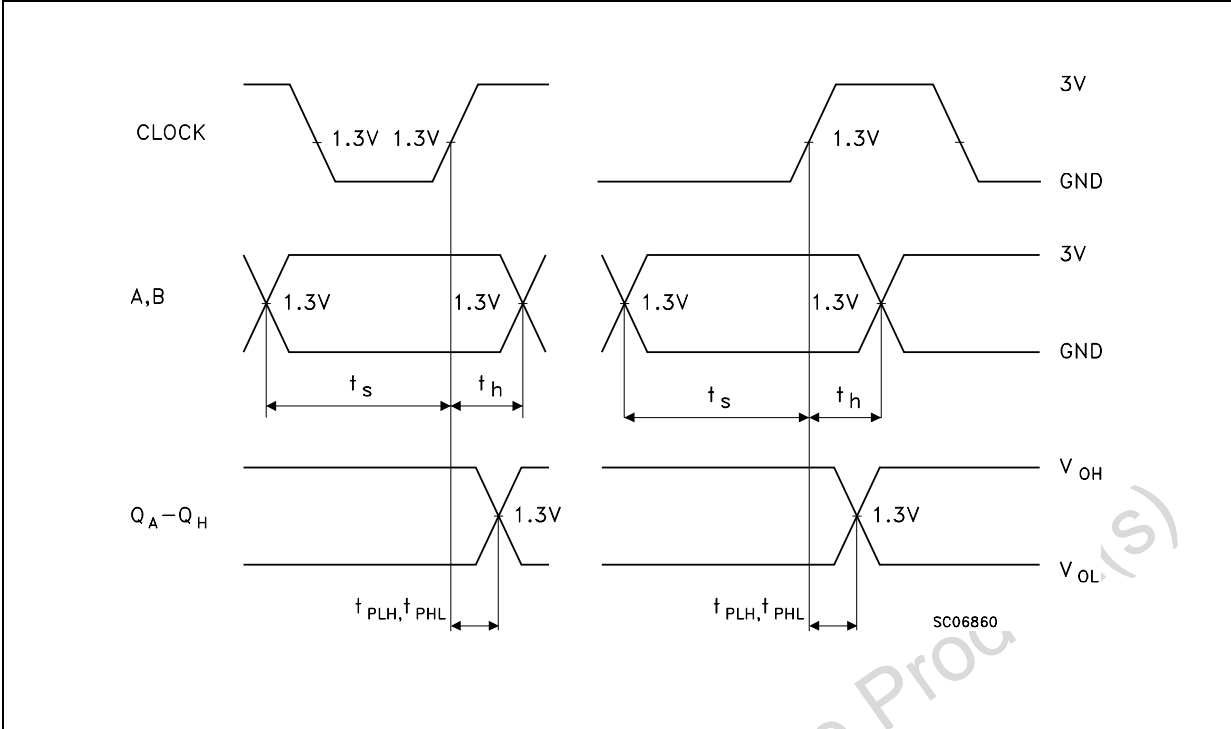


$C_L = 50\text{pF}$  or equivalent (includes jig and probe capacitance)  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

**WAVEFORM 1 : MINIMUM PULSE WIDTH (CLEAR) AND REMOVAL TIME( CLEAR TO CLOCK)**  
 (f=1MHz; 50% duty cycle)

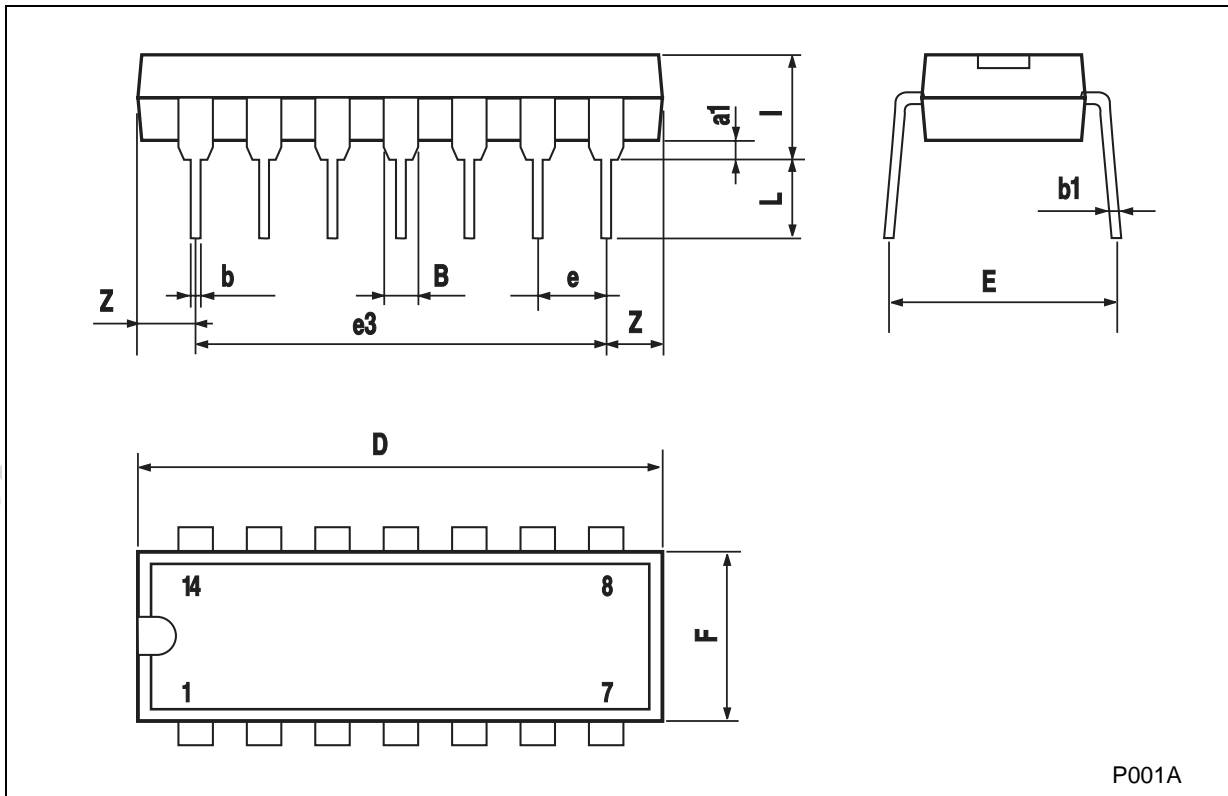


WAVEFORM 2 : PROPAGATION DELAY TIMES, SETUP AND HOLD TIME (f=1MHz; 50% duty cycle)



**Plastic DIP-14 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

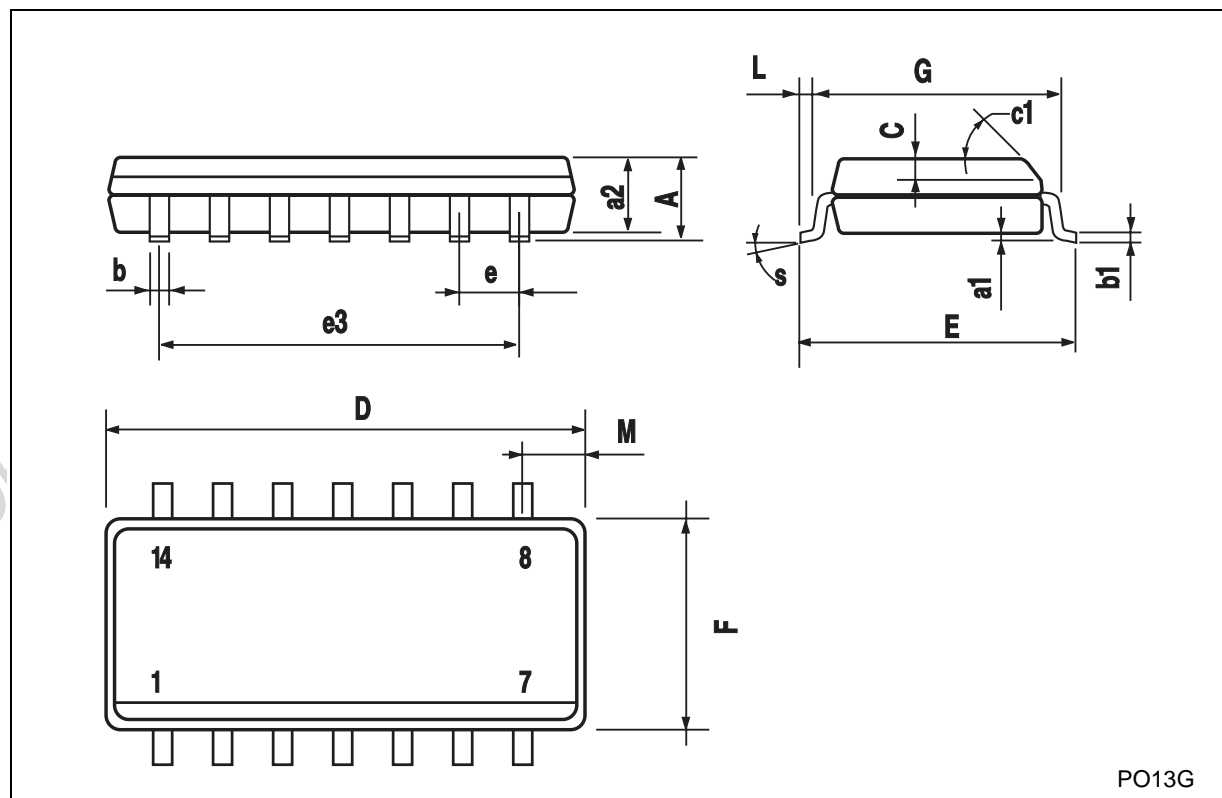


P001A



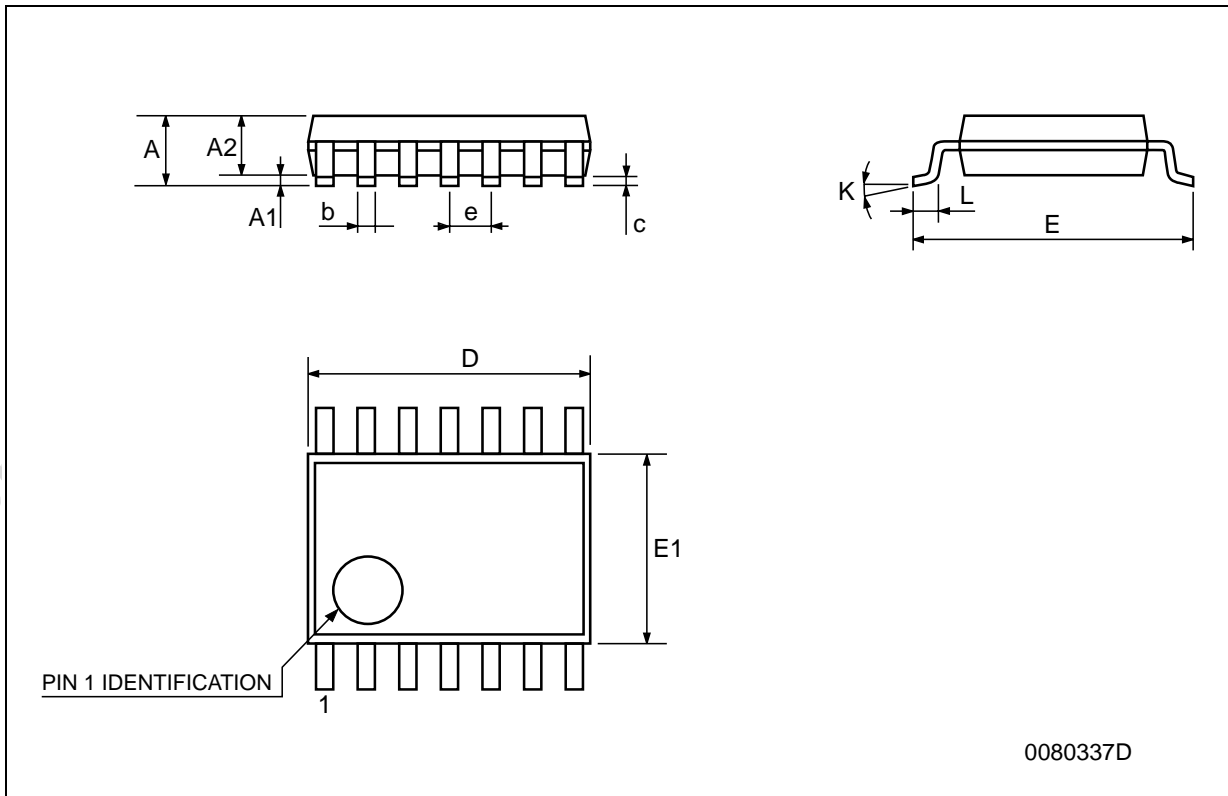
## SO-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					



**TSSOP14 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



Obsolete Product(s) - Obsolete Product(s)

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2001 STMicroelectronics - Printed in Italy - All Rights Reserved  
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco  
Singapore - Spain - Sweden - Switzerland - United Kingdom

© <http://www.st.com>

