19-2930; Rev 0; 8/03

500MHz to 1100MHz Adjustable RF Predistorter

General Description

The MAX2010 adjustable RF predistorter is designed to improve power amplifier (PA) adjacent-channel power rejection (ACPR) by introducing gain and phase expansion in a PA chain to compensate for the PA's gain and phase compression. With its +23dBm maximum input power level and wide adjustable range, the MAX2010 can provide up to 12dB of ACPR improvement for power amplifiers operating in the 500MHz to 1100MHz frequency band. Higher frequencies of operation can be achieved with this IC's counterpart, the MAX2009.

The MAX2010 is unique in that it provides up to 6dB of gain expansion and 21° of phase expansion as the input power is increased. The amount of expansion is configurable through two independent sets of control: one set adjusts the gain expansion breakpoint and slope, while the second set controls the same parameters for phase. With these settings in place, the linearization circuit can be run in either a static set-and-forget mode, or a more sophisticated closed-loop implementation can be employed with real-time software-controlled distortion correction. Hybrid correction modes are also possible using simple lookup tables to compensate for factors such as PA temperature drift or PA loading.

The MAX2010 comes in a 28-pin thin QFN exposed pad (EP) package (5mm x 5mm) and is specified for the extended (-40°C to +85°C) temperature range.

Applications

cdma2000™, GSM/EDGE, and iDEN Base Stations

Feed-Forward PA Architectures

Digital Baseband Predistortion Architectures

Military Applications

cdma2000 is a trademark of Telecommunications Industry Assoc.

Features

- **Up to 12dB ACPR Improvement***
- **Independent Gain and Phase Expansion Controls**
- **Gain Expansion Up to 6dB**
- **Phase Expansion Up to 21°**
- **500MHz to 1100MHz Frequency Range**
- **Exceptional Gain and Phase Flatness**
- **Group Delay <2.4ns (Gain and Phase Sections Combined)**
- **±0.03ns Group Delay Ripple Over a 100MHz Band**
- **Capable of Handling Input Drives Up to +23dBm**
- **On-Chip Temperature Variation Compensation**
- **Single +5V Supply**
- **Low Power Consumption: 75mW (typ)**
- **Fully Integrated into Small 28-Pin Thin QFN Package**

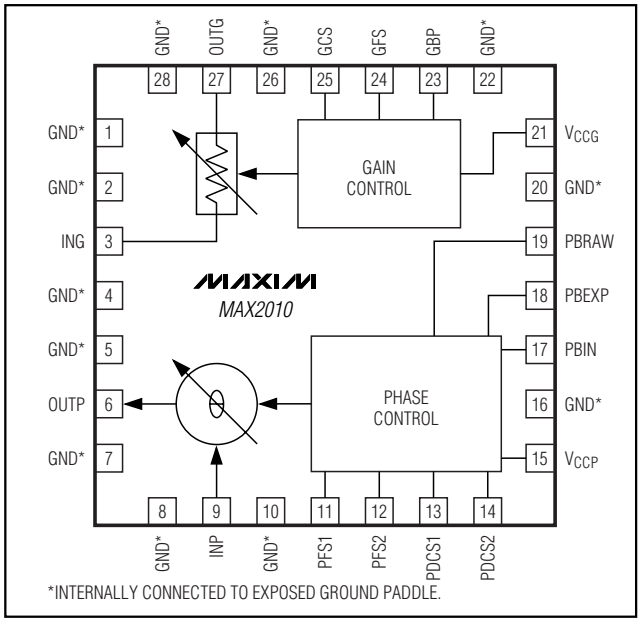
**Performance dependent on amplifier, bias, and modulation.*

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2010ETI-T	-40°C to +85°C	28 Thin QFN-EP*

**EP = Exposed paddle.*

Functional Diagram/ Pin Configuration



500MHz to 1100MHz Adjustable RF Predistorter

ABSOLUTE MAXIMUM RATINGS

V_{CCG}, V_{CCP} to GND .....-0.3V to +5.5V
ING, OUTG, GCS, GFS, GBP to GND.....-0.3V to (V_{CCG} + 0.3V)
INP, OUTP, PFS_, PDCS_, PBRAW,
PBEXP, PBIN to GND .....-0.3V to (V_{CCP} + 0.3V)
Input (ING, INP, OUTP, OUTG) Level .....+23dBm
PBEXP Output Current .....±1mA

Continuous Power Dissipation (T_A = +70°C)
28-Pin Thin QFN-EP
(derate 21mW/°C above +70°C).....1667mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(MAX2010 EV kit; V_{CCG} = V_{CCP} = +4.75V to +5.25V; no RF signal applied; INP, ING, OUTP, OUTG are AC-coupled and terminated to 50Ω. V_{PF_S1} = open; PBEXP shorted to PBRAW; V_{PDCS1} = V_{PDCS2} = 0.8V; V_{PBIN} = V_{GBP} = V_{GCS} = GND; V_{GFS} = V_{CCG}; T_A = -40°C to +85°C. Typical values are at V_{CCG} = V_{CCP} = +5.0V, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CCG}, V_{CCP}	4.75		5.25	V
Supply Current	V_{CCP}		5.8	7	mA
	V_{CCG}		10	12.1	
Analog Input Voltage Range	PBIN, PBRAW	0		V_{CCP}	V
	GBP, GFS, GCS	0		V_{CCG}	
Analog Input Current	V_{GFS} = V_{GCS} = V_{PBRAW} = 0V	-2		+2	µA
	V_{GBP} = 0 to +5V	-100		+170	
	V_{PBIN} = 0 to +5V	-100		+220	
Logic-Input High Voltage	PDCS1, PDCS2 (Note 1)	2.0			V
Logic-Input Low Voltage	PDCS1, PDCS2 (Note 1)			0.8	V
Logic Input Current		-2		+2	µA

AC ELECTRICAL CHARACTERISTICS

(MAX2010 EV kit, V_{CCG} = V_{CCP} = +4.75V to +5.25V, 50Ω environment, P_{IN} = -20dBm, f_{IN} = 500MHz to 1100MHz, V_{GCS} = +1.0V, V_{GFS} = +5.0V, V_{GBP} = +1.2V, V_{PBIN} = V_{PDCS1} = V_{PDCS2} = 0V, V_{PF_S1} = +5V, V_{PBRAW} = V_{PBEXP}, T_A = -40°C to +85°C. Typical values are at f_{IN} = 880MHz, V_{CCG} = V_{CCP} = +5V, T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Frequency Range		500		1100	MHz
VSWR	ING, INP, OUTG, OUTP		1.3:1		
PHASE CONTROL SECTION					
Nominal Gain			-5.5		dB
Gain Variation Over Temperature	T_A = -40°C to +85°C		-1.7		dB
Gain Flatness	Over a 100MHz band		±0.1		dB
Phase-Expansion Breakpoint Maximum	V_{PBIN} = +5V		23		dBm
Phase-Expansion Breakpoint Minimum	V_{PBIN} = 0V		0.7		dBm
Phase-Expansion Breakpoint Variation Over Temperature	T_A = -40°C to +85°C		±1.5		dB
Phase Expansion	V_{PF_S1} = +5V, V_{PDCS1} = V_{PDCS2} = 0V, P_{IN} = -20 dBm to +23 dBm		21		Degrees
	V_{PDCS1} = 5V, V_{PDCS2} = 0V, V_{PF_S1} = +1.5V		16		
	V_{PDCS1} = 0V, V_{PDCS2} = 5V, V_{PF_S1} = +1.5V		14		
	V_{PF_S1} = 0V, V_{PDCS1} = V_{PDCS2} = +5V, P_{IN} = -20dBm to +23dBm		6		
Phase-Expansion Slope Maximum	P_{IN} = +9dBm		1.4		Degrees /dB
Phase-Expansion Slope Minimum	V_{PF_S1} = 0V, V_{PDCS1} = V_{PDCS2} = +5V, P_{IN} = +9dBm		0.6		Degrees /dB
Phase-Slope Variation Over Temperature	P_{IN} = +9dBm, T_A = -40°C to +85°C		0.05		Degrees /dB
Phase Ripple	Over a 100MHz band, deviation from linear phase		±0.02		Degrees
Noise Figure			5.5		dB
Absolute Group Delay	Interconnects de-embedded		1.3		ns
Group Delay Ripple	Over a 100MHz band		±0.01		ns
Parasitic Gain Expansion	P_{IN} = -20dBm to +23dBm		+0.4		dB

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AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2010 EV kit, V_{CCG} = V_{CCP} = +4.75V to +5.25V, 50Ω environment, P_{IN} = -20dBm, f_{IN} = 500MHz to 1100MHz, V_{GCS} = +1.0V, V_{GFS} = +5.0V, V_{GBP} = +1.2V, V_{PBIN} = V_{PDCS1} = V_{PDCS2} = 0V, V_{PF_S1} = +5V, V_{PBRAW} = V_{PBEXP}, T_A = -40°C to +85°C. Typical values are at f_{IN} = 880MHz, V_{CCG} = V_{CCP} = +5V, T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GAIN CONTROL SECTION					
Nominal Gain			-14.9		dB
	V_{GCS} = 0V, V_{GFS} = +5V		-24.3		
	V_{GCS} = +5V, V_{GFS} = 0V		-7.6		
Gain Variation Over Temperature	T_A = -40°C to +85°C		-1.4		dB
Gain Flatness	Over a 100MHz band		±0.2		dB
Gain-Expansion Breakpoint Maximum	V_{GBP} = +5V		23		dBm
Gain-Expansion Breakpoint Minimum	V_{GBP} = +0.5V		-2.5		dBm
Gain-Expansion Breakpoint Variation Over Temperature	T_A = -40°C to +85°C		-0.5		dB
Gain-Expansion	V_{GFS} = +5V, P_{IN} = -20dBm to +23dBm		5.3		dB
	V_{GFS} = 0V, P_{IN} = -20dBm to +23dBm		3.1		
Gain-Expansion Slope	V_{GFS} = +5V, P_{IN} = +15dBm		0.43		dB/dB
	V_{GFS} = +0V, P_{IN} = +15dBm		0.23		
Gain-Slope Variation Over Temperature	P_{IN} = +15dBm, T_A = -40°C to +85°C		-0.01		dB/dB
Noise Figure			14.9		dB
Absolute Group Delay	Interconnects de-embedded		1.12		ns
Group Delay Ripple	Over a 100MHz band		±0.02		ns
Phase Ripple	Over a 100MHz band, deviation from linear phase		±0.09		Degrees
Parasitic Phase Expansion	P_{IN} = -20dBm to +23dBm		+3		Degrees

Note 1: Guaranteed by design and characterization.

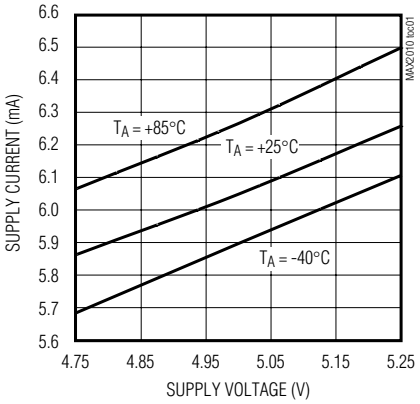
Note 2: All limits reflect losses and characteristics of external components shown in the *Typical Application Circuit*, unless otherwise noted.

Typical Operating Characteristics

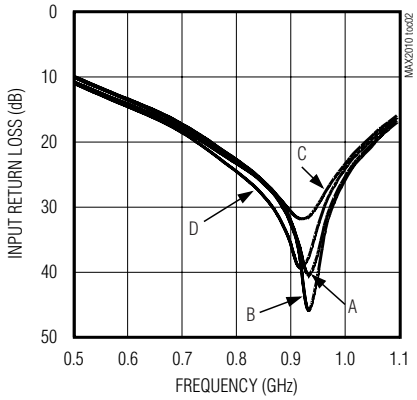
Phase Control Section

(MAX2010 EV kit, V_{CCP} = +5.0V, P_{IN} = -20dBm, V_{PBIN} = 0V, V_{PF_S1} = +5.0V, V_{PDCS1} = V_{PDCS2} = 0V, f_{IN} = 880MHz, T_A = +25°C unless otherwise noted.)

SUPPLY CURRENT vs. SUPPLY VOLTAGE

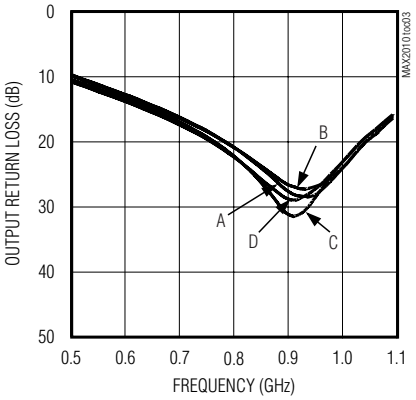


SMALL-SIGNAL INPUT RETURN LOSS vs. FREQUENCY



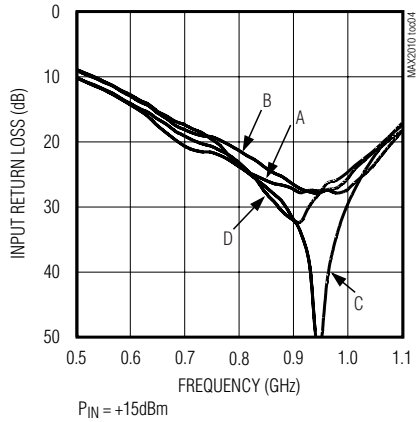
A = V_{PDCS1} = V_{PDCS2} = V_{PF_S1} = 0V
B = V_{PDCS1} = V_{PDCS2} = 0V, V_{PF_S1} = 5V
C = V_{PDCS1} = V_{PDCS2} = 5V, V_{PF_S1} = 0V
D = V_{PDCS1} = V_{PDCS2} = V_{PF_S1} = 5V

SMALL-SIGNAL OUTPUT RETURN LOSS vs. FREQUENCY



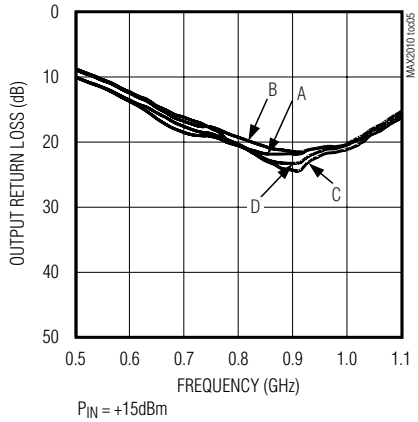
A = V_{PDCS1} = V_{PDCS2} = V_{PF_S1} = 0V
B = V_{PDCS1} = V_{PDCS2} = 0V, V_{PF_S1} = 5V
C = V_{PDCS1} = V_{PDCS2} = 5V, V_{PF_S1} = 0V
D = V_{PDCS1} = V_{PDCS2} = V_{PF_S1} = 5V

LARGE-SIGNAL INPUT RETURN LOSS vs. FREQUENCY



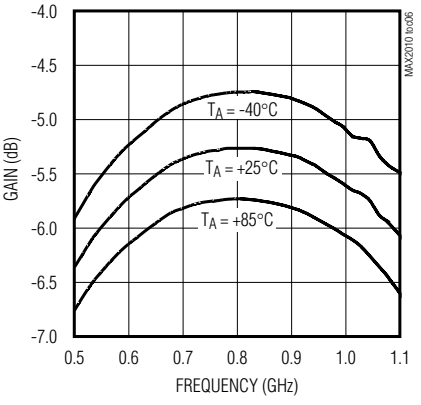
P_{IN} = +15dBm
A = V_{PDCS1} = V_{PDCS2} = V_{PF_S1} = 0V
B = V_{PDCS1} = V_{PDCS2} = 0V, V_{PF_S1} = 5V
C = V_{PDCS1} = V_{PDCS2} = 5V, V_{PF_S1} = 0V
D = V_{PDCS1} = V_{PDCS2} = V_{PF_S1} = 5V

LARGE-SIGNAL OUTPUT RETURN LOSS vs. FREQUENCY



P_{IN} = +15dBm
A = V_{PDCS1} = V_{PDCS2} = V_{PF_S1} = 0V
B = V_{PDCS1} = V_{PDCS2} = 0V, V_{PF_S1} = 5V
C = V_{PDCS1} = V_{PDCS2} = 5V, V_{PF_S1} = 0V
D = V_{PDCS1} = V_{PDCS2} = V_{PF_S1} = 5V

SMALL-SIGNAL GAIN vs. FREQUENCY



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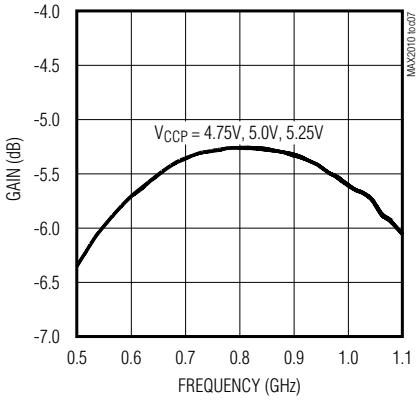
Typical Operating Characteristics (continued)

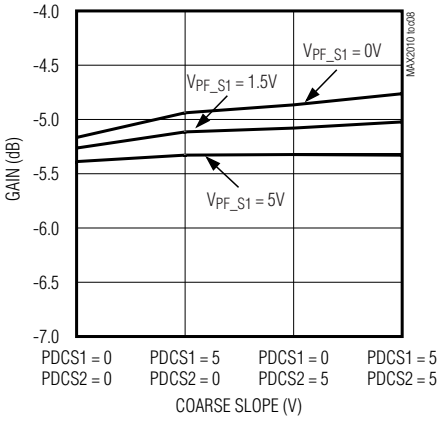
Phase Control Section (continued)

(MAX2010 EV kit, V_{CCP} = +5.0V, P_{IN} = -20dBm, V_{PBIN} = 0V, V_{PF_S1} = +5.0V, V_{PDCS1} = V_{PDCS2} = 0V, f_{IN} = 880MHz, T_A = +25°C unless otherwise noted.)

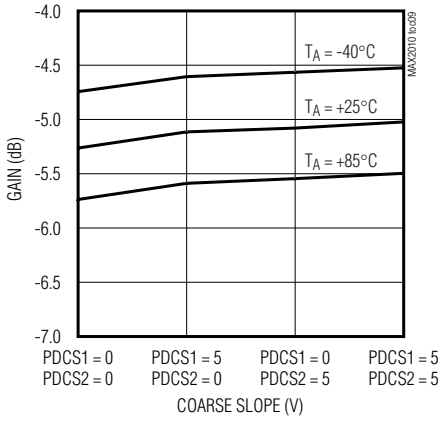
SMALL-SIGNAL GAIN vs. FREQUENCY



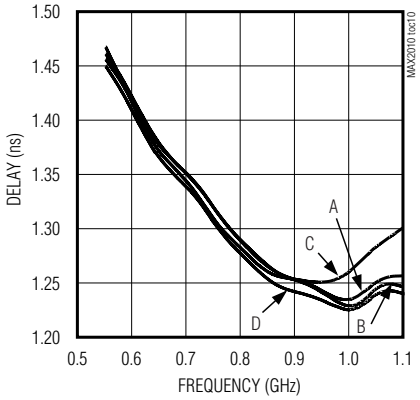
SMALL-SIGNAL GAIN vs. COARSE SLOPE



SMALL-SIGNAL GAIN vs. COARSE SLOPE

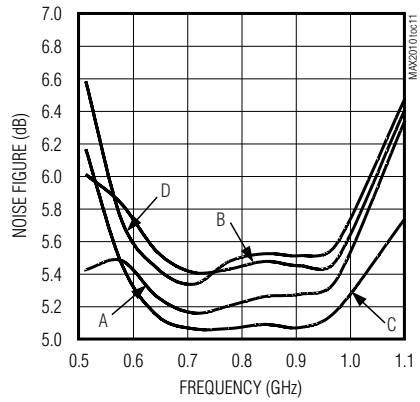


GROUP DELAY vs. FREQUENCY



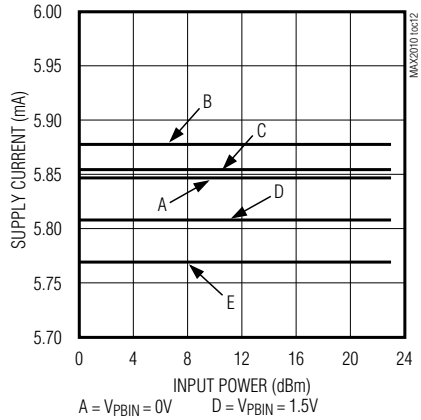
A = V_{PDCS1} = V_{PDCS2} = V_{PF_S1} = 0V
B = V_{PDCS1} = V_{PDCS2} = 0V, V_{PF_S1} = 5V
C = V_{PDCS1} = V_{PDCS2} = 5V, V_{PF_S1} = 0V
D = V_{PDCS1} = V_{PDCS2} = V_{PF_S1} = 5V
INTERCONNECTS DE-EMBEDDED

NOISE FIGURE vs. FREQUENCY



A = V_{PDCS1} = V_{PDCS2} = V_{PF_S1} = 0V
B = V_{PDCS1} = V_{PDCS2} = 0V, V_{PF_S1} = 5V
C = V_{PDCS1} = V_{PDCS2} = 5V, V_{PF_S1} = 0V
D = V_{PDCS1} = V_{PDCS2} = V_{PF_S1} = 5V

SUPPLY CURRENT vs. INPUT POWER



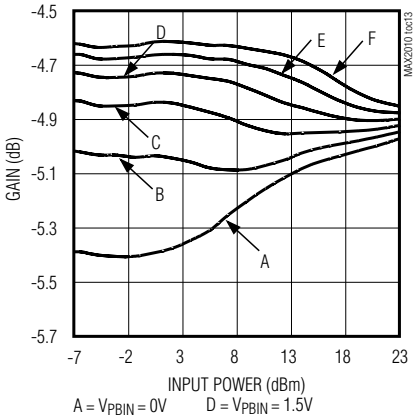
A = V_{PBIN} = 0V
B = V_{PBIN} = 0.5V
C = V_{PBIN} = 1.0V
D = V_{PBIN} = 1.5V
E = V_{PBIN} = 3.0V

Typical Operating Characteristics (continued)

Phase Control Section (continued)

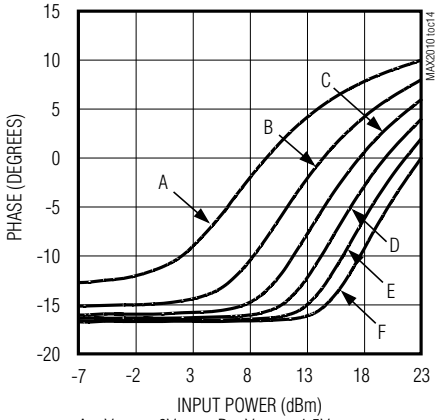
(MAX2010 EV kit, V_{CCP} = +5.0V, P_{IN} = -20dBm, V_{PBIN} = 0V, V_{PF_S1} = +5.0V, V_{PDCS1} = V_{PDCS2} = 0V, f_{IN} = 880MHz, T_A = +25°C unless otherwise noted.)

GAIN EXPANSION vs. INPUT POWER



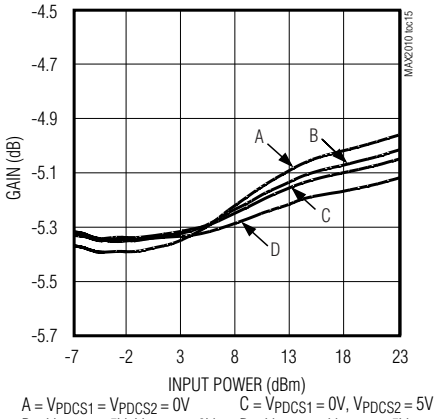
A = V_{PBIN} = 0V D = V_{PBIN} = 1.5V
B = V_{PBIN} = 0.5V E = V_{PBIN} = 2.0V
C = V_{PBIN} = 1.0V F = V_{PBIN} = 2.5V

PHASE EXPANSION vs. INPUT POWER



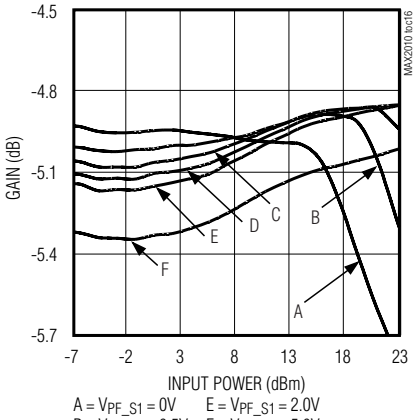
A = V_{PBIN} = 0V D = V_{PBIN} = 1.5V
B = V_{PBIN} = 0.5V E = V_{PBIN} = 2.0V
C = V_{PBIN} = 1.0V F = V_{PBIN} = 2.5V

GAIN EXPANSION vs. INPUT POWER



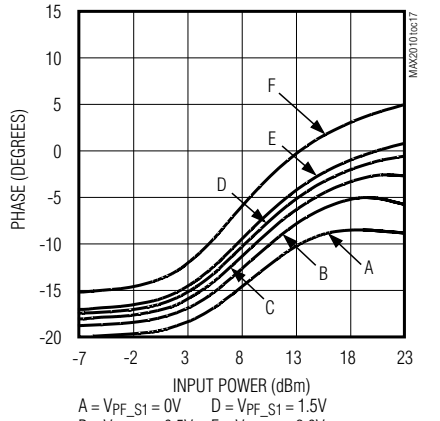
A = V_{PDCS1} = V_{PDCS2} = 0V C = V_{PDCS1} = 0V, V_{PDCS2} = 5V
B = V_{PDCS1} = 5V, V_{PDCS2} = 0V D = V_{PDCS1} = V_{PDCS2} = 5V

GAIN EXPANSION vs. INPUT POWER



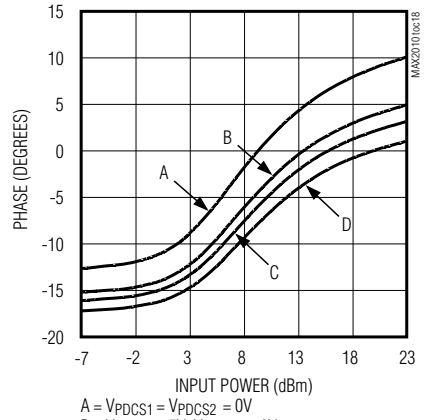
A = V_{PF_S1} = 0V E = V_{PF_S1} = 2.0V
B = V_{PF_S1} = 0.5V F = V_{PF_S1} = 5.0V
C = V_{PF_S1} = 1.0V V_{PDCS1} = 5.0V
D = V_{PF_S1} = 1.5V

PHASE EXPANSION vs. INPUT POWER



A = V_{PF_S1} = 0V D = V_{PF_S1} = 1.5V
B = V_{PF_S1} = 0.5V E = V_{PF_S1} = 2.0V
C = V_{PF_S1} = 1.0V F = V_{PF_S1} = 5.0V
V_{PDCS1} = 5.0V

PHASE EXPANSION vs. INPUT POWER



A = V_{PDCS1} = V_{PDCS2} = 0V
B = V_{PDCS1} = 5V, V_{PDCS2} = 0V
C = V_{PDCS1} = 0V, V_{PDCS2} = 5V
D = V_{PDCS1} = V_{PDCS2} = 5V

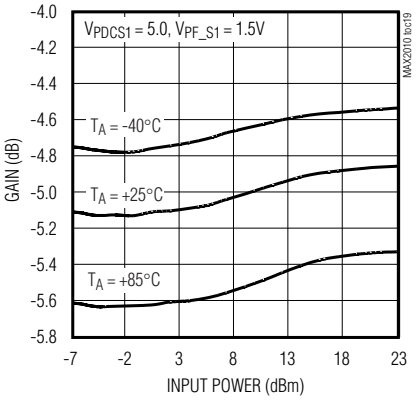
500MHz to 1100MHz Adjustable RF Predistorter

Typical Operating Characteristics (continued)

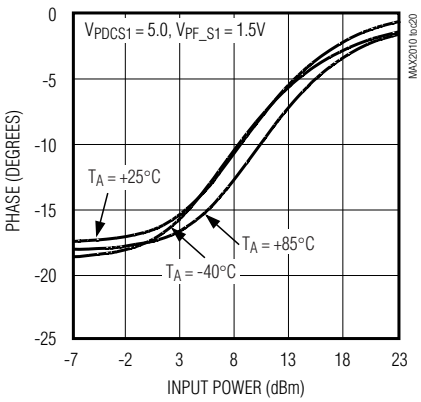
Phase Control Section (continued)

(MAX2010 EV kit, V_{CCP} = +5.0V, P_{IN} = -20dBm, V_{PBIN} = 0V, V_{PF_S1} = +5.0V, V_{PDCS1} = V_{PDCS2} = 0V, f_{IN} = 880MHz, T_A = +25°C unless otherwise noted.)

GAIN EXPANSION vs. INPUT POWER



PHASE EXPANSION vs. INPUT POWER

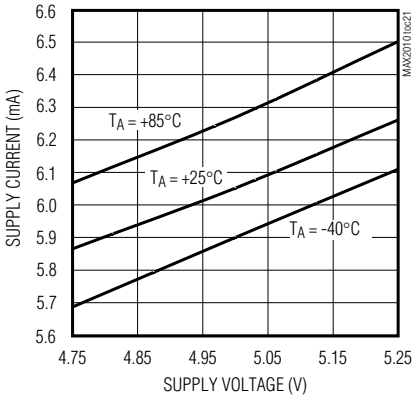


Typical Operating Characteristics

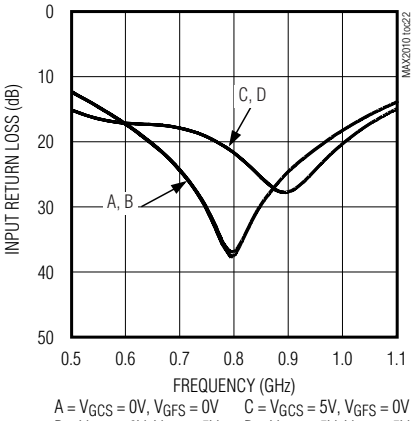
Gain Control Section

(MAX2010 EV kit, V_{CCG} = +5.0V, P_{IN} = -20dBm, V_{GBP} = +1.2V, V_{GFS} = +5.0V, V_{GCS} = +1.0V, f_{IN} = 880MHz, T_A = +25°C, unless otherwise noted.)

SUPPLY CURRENT vs. SUPPLY VOLTAGE

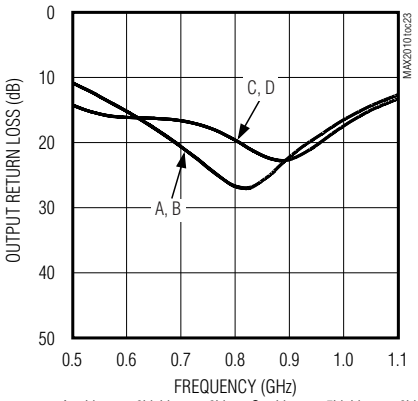


SMALL-SIGNAL INPUT RETURN LOSS vs. FREQUENCY



A = V_{GCS} = 0V, V_{GFS} = 0V C = V_{GCS} = 5V, V_{GFS} = 0V
B = V_{GCS} = 0V, V_{GFS} = 5V D = V_{GCS} = 5V, V_{GFS} = 5V

SMALL-SIGNAL OUTPUT RETURN LOSS vs. FREQUENCY



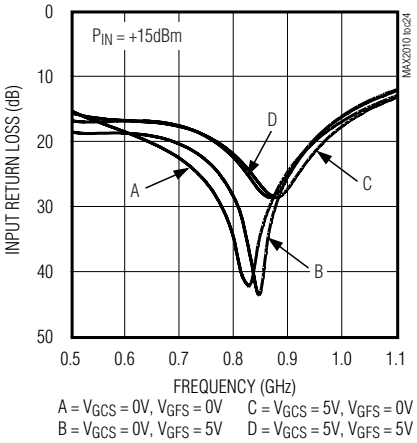
A = V_{GCS} = 0V, V_{GFS} = 0V C = V_{GCS} = 5V, V_{GFS} = 0V
B = V_{GCS} = 0V, V_{GFS} = 5V D = V_{GCS} = 5V, V_{GFS} = 5V

Typical Operating Characteristics (continued)

Gain Control Section (continued)

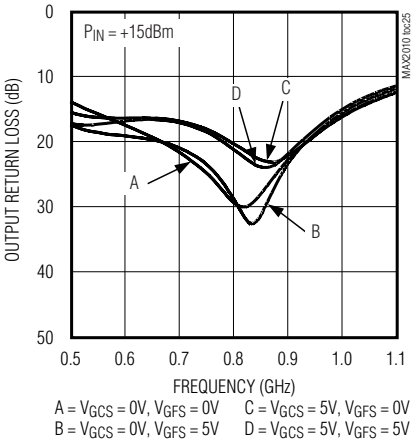
(MAX2010 EV kit, V_{CCP} = +5.0V, P_{IN} = -20dBm, V_{PBIN} = 0V, V_{PF_S1} = +5.0V, V_{PDCS1} = V_{PDCS2} = 0V, f_{IN} = 880MHz, T_A = +25°C unless otherwise noted.)

LARGE-SIGNAL INPUT RETURN LOSS vs. FREQUENCY



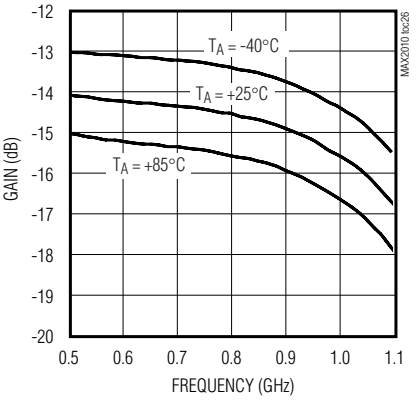
A = V_{GCS} = 0V, V_{GFS} = 0V C = V_{GCS} = 5V, V_{GFS} = 0V
B = V_{GCS} = 0V, V_{GFS} = 5V D = V_{GCS} = 5V, V_{GFS} = 5V

LARGE-SIGNAL OUTPUT RETURN LOSS vs. FREQUENCY

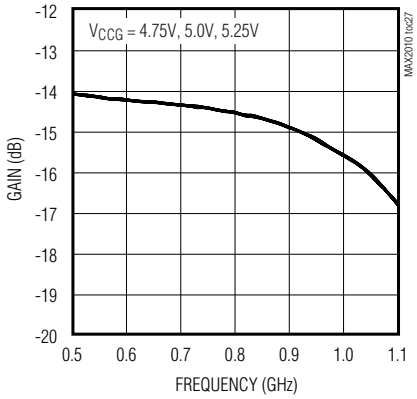


A = V_{GCS} = 0V, V_{GFS} = 0V C = V_{GCS} = 5V, V_{GFS} = 0V
B = V_{GCS} = 0V, V_{GFS} = 5V D = V_{GCS} = 5V, V_{GFS} = 5V

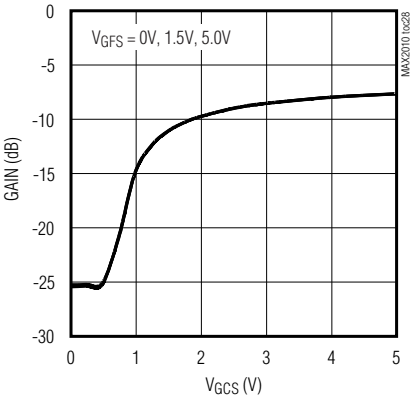
SMALL-SIGNAL GAIN vs. FREQUENCY



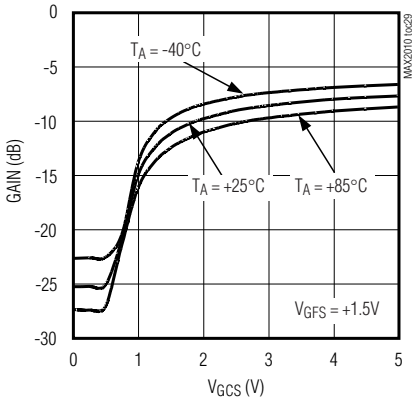
SMALL-SIGNAL GAIN vs. FREQUENCY



SMALL-SIGNAL GAIN vs. V_{GCS}



SMALL-SIGNAL GAIN vs. V_{GCS}



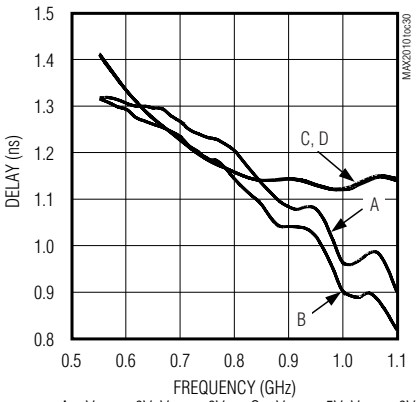
500MHz to 1100MHz Adjustable RF Predistorter

Typical Operating Characteristics (continued)

Gain Control Section (continued)

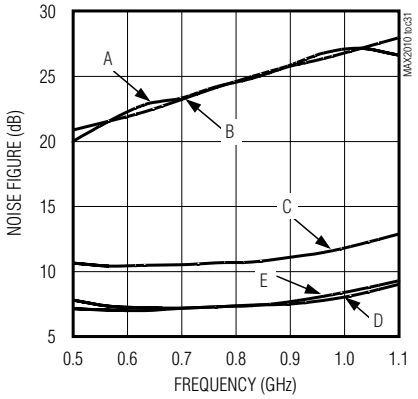
(MAX2010 EV kit, V_{CCP} = +5.0V, P_{IN} = -20dBm, V_{PBIN} = 0V, V_{PF_S1} = +5.0V, V_{PDCS1} = V_{PDCS2} = 0V, f_{IN} = 880MHz, T_A = +25°C unless otherwise noted.)

GROUP DELAY vs. FREQUENCY



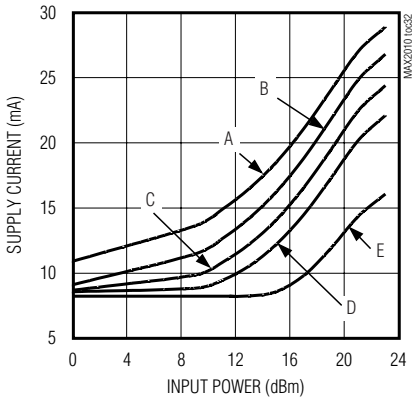
A = V_{GCS} = 0V, V_{GFS} = 0V C = V_{GCS} = 5V, V_{GFS} = 0V
B = V_{GCS} = 0V, V_{GFS} = 5V D = V_{GCS} = 5V, V_{GFS} = 5V
INTERCONNECTS DE-EMBEDDED

NOISE FIGURE vs. FREQUENCY



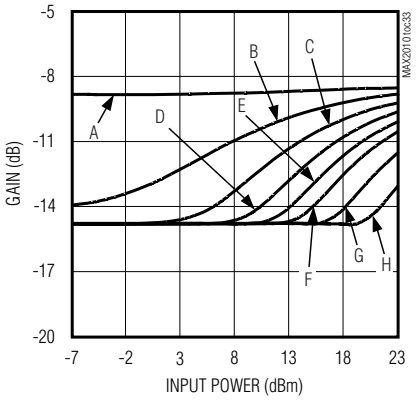
A = V_{GCS} = 0V, V_{GFS} = 0V D = V_{GCS} = 5V, V_{GFS} = 0V
B = V_{GCS} = 0V, V_{GFS} = 5V E = V_{GCS} = 5V, V_{GFS} = 5V
C = V_{GCS} = 1.5V, V_{GFS} = 5V

SUPPLY CURRENT vs. INPUT POWER



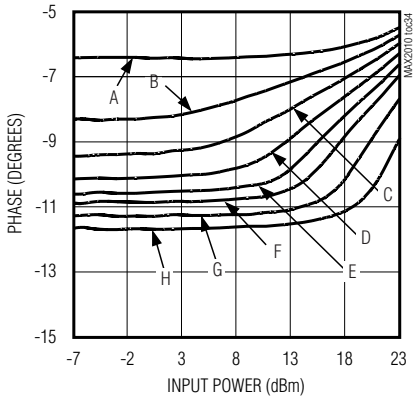
A = V_{GBP} = 0V D = V_{GBP} = 1.5V
B = V_{GBP} = 0.5V E = V_{GBP} = 3.0V
C = V_{GBP} = 1.0V

GAIN EXPANSION vs. INPUT POWER



A = V_{GBP} = 0V E = V_{GBP} = 2.0V
B = V_{GBP} = 0.5V F = V_{GBP} = 2.5V
C = V_{GBP} = 1.0V G = V_{GBP} = 3.5V
D = V_{GBP} = 1.5V H = V_{GBP} = 5.0V

PHASE EXPANSION vs. INPUT POWER



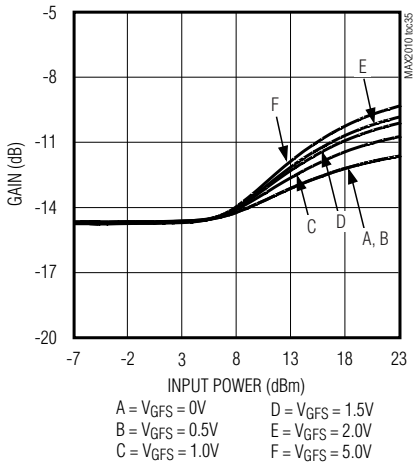
A = V_{GBP} = 0V E = V_{GBP} = 2.0V
B = V_{GBP} = 0.5V F = V_{GBP} = 2.5V
C = V_{GBP} = 1.0V G = V_{GBP} = 3.5V
D = V_{GBP} = 1.5V H = V_{GBP} = 5.0V

Typical Operating Characteristics (continued)

Gain Control Section (continued)

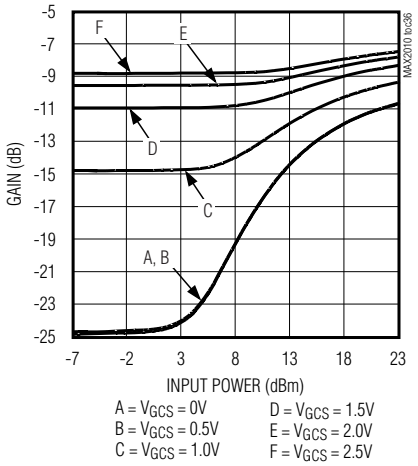
(MAX2010 EV kit, V_{CCP} = +5.0V, P_{IN} = -20dBm, V_{PBIN} = 0V, V_{PF_S1} = +5.0V, V_{PDCS1} = V_{PDCS2} = 0V, f_{IN} = 880MHz, T_A = +25°C unless otherwise noted.)

GAIN EXPANSION vs. INPUT POWER



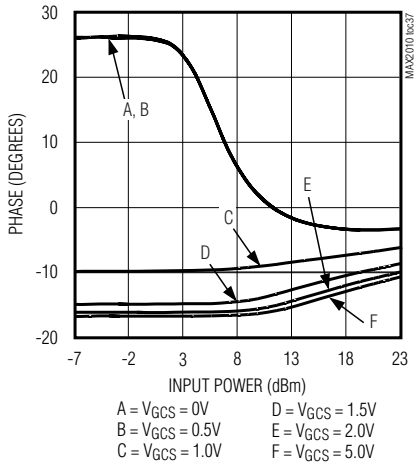
A = V_{GFS} = 0V
B = V_{GFS} = 0.5V
C = V_{GFS} = 1.0V
D = V_{GFS} = 1.5V
E = V_{GFS} = 2.0V
F = V_{GFS} = 5.0V

GAIN EXPANSION vs. INPUT POWER



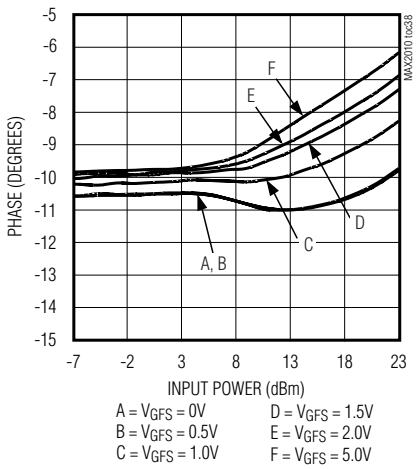
A = V_{GCS} = 0V
B = V_{GCS} = 0.5V
C = V_{GCS} = 1.0V
D = V_{GCS} = 1.5V
E = V_{GCS} = 2.0V
F = V_{GCS} = 2.5V

PHASE EXPANSION vs. INPUT POWER



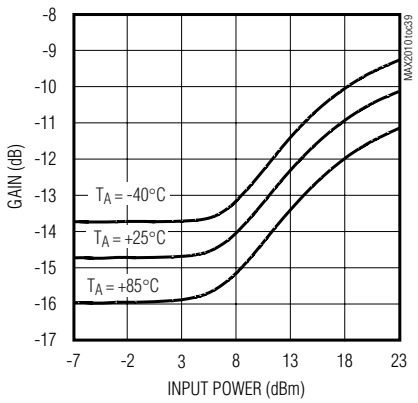
A = V_{GCS} = 0V
B = V_{GCS} = 0.5V
C = V_{GCS} = 1.0V
D = V_{GCS} = 1.5V
E = V_{GCS} = 2.0V
F = V_{GCS} = 5.0V

PHASE EXPANSION vs. INPUT POWER

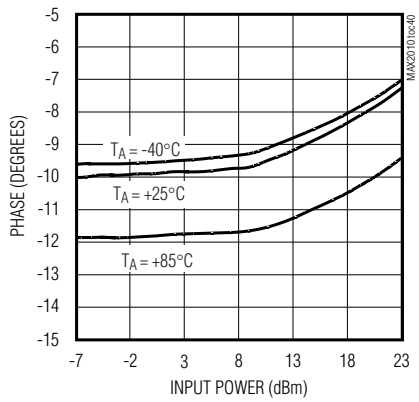


A = V_{GFS} = 0V
B = V_{GFS} = 0.5V
C = V_{GFS} = 1.0V
D = V_{GFS} = 1.5V
E = V_{GFS} = 2.0V
F = V_{GFS} = 5.0V

GAIN EXPANSION vs. INPUT POWER



PHASE EXPANSION vs. INPUT POWER



500MHz to 1100MHz Adjustable RF Predistorter

Pin Description

PIN	NAME	FUNCTION
1, 2, 4, 5, 7, 8, 10, 16, 20, 22, 26, 28	GND	Ground. Internally connected to the exposed paddle.
3	ING	RF Gain Input. Connect ING to a coupling capacitor if it is not connected to OUTP. ING is interchangeable with OUTG.
6	OUTP	RF Phase Output. Connect OUTP to a coupling capacitor if it is not connected to INP. OUTP is interchangeable with INP.
9	INP	RF Phase Input. Connect INP to a coupling capacitor. This pin is interchangeable with OUTP.
11	PFS1	Fine Phase-Slope Control Input 1. See the *Typical Application Circuit*.
12	PFS2	Fine Phase-Slope Control Input 2. See the *Typical Application Circuit*.
13	PDCS1	Digital Coarse Phase-Slope Control Range Input 1. Set to logical zero for the steepest slope.
14	PDCS2	Digital Coarse Phase-Slope Control Range Input 2. Set to logical zero for the steepest slope.
15	V_{CCP}	Phase-Control Supply Voltage. Bypass with a 0.01µF capacitor to ground as close to the device as possible. Phase section can operate without V_{CCG}.
17	PBIN	Phase Breakpoint Control Input
18	PBEXP	Phase Expansion Output. Connect PBEXP to PBRAW to use PBIN as the breakpoint control voltage.
19	PBRAW	Uncompensated Phase Breakpoint Input
21	V_{CCG}	Gain-Control Supply Voltage. Bypass with a 0.01µF capacitor to ground as close to the device as possible. Gain section can operate without V_{CCP}.
23	GBP	Gain Breakpoint Control Input
24	GFS	Fine Gain-Slope Control Input
25	GCS	Coarse Gain-Slope Control Input
27	OUTG	RF Gain Output. Connect OUTG to a coupling capacitor. OUTG is interchangeable with ING.
EP	GND	Exposed Ground Paddle. Solder EP to the ground plane.

Detailed Description

The MAX2010 adjustable predistorter can provide up to 12dB of ACPR improvement for high-power amplifiers by introducing gain and phase expansion to compensate for the PA's gain and phase compression. The MAX2010 enables real-time software-controlled distortion correction, as well as set-and-forget tuning through the adjustment of the expansion starting point (breakpoint) and the rate of expansion (slope). The gain and phase breakpoints can be set over a 20dB input power range. The phase expansion slope is variable from 0.3°/dB to 2.0°/dB and can be adjusted for a maximum of 21° of phase expansion. The gain expansion slope is variable from 0.1dB/dB to 0.53dB/dB and can be adjusted for a maximum of 6dB gain expansion.

The following sections describe the tuning methodology best implemented with a class A amplifier. Other classes of operation may require significantly different settings.

Phase Expansion Circuitry

Figure 1 shows a typical PA's phase behavior with respect to input power. For input powers less than the breakpoint level, the phase remains relatively constant. As the input power becomes greater than the breakpoint level, the phase begins to compress and deteriorate the power amplifier's linearity. To compensate for this AM-PM distortion, the MAX2010 provides phase expansion, which occurs at the same breakpoint level but with the opposite slope. The overall result is a flat phase response.

Phase Expansion Breakpoint

The phase expansion breakpoint is typically controlled by a digital-to-analog converter (DAC) connected through the PBIN pin. The PBIN input voltage range of 0V to V_{CC} corresponds to a breakpoint input power range of 0.7dBm to 23dBm. To achieve optimal performance, the phase expansion breakpoint of the MAX2010 must be set to equal the phase compression breakpoint of the PA.

Phase Expansion Slope

The phase expansion slope of the MAX2010 must also be adjusted to equal the opposite slope of the PA's phase compression curve. The phase expansion slope of the MAX2010 is controlled by the PFS1, PFS2, PDCS1, and PDCS2 pins. With pins PFS1 and PFS2 AC-coupled and connected to a variable capacitor or varactor diode, the PFS1 and PFS2 pins perform the task of fine tuning the phase expansion slope. Since off-chip varactor diodes are recommended for this function, they must be closely matched and identically biased. A minimum effective capacitance of 2pF to 6pF is required to achieve the full phase slope range as specified in the *Electrical Characteristics* tables.

As shown in Figure 2, the varactors connected to PFS1 and PFS2 are in series with three internal capacitors on each pin. By connecting and disconnecting these internal capacitors, a larger change in phase expansion slope can be achieved through the logic levels presented at the PDCS1 and PDCS2 pins. The phase expansion slope is at its maximum when both V_{PDCS1} and V_{PDCS2} equal 0V. The phase tuning has a minimal effect on the small-signal gain.

Gain Expansion Circuitry

In addition to phase compression, the PA also suffers from gain compression (AM-AM) distortion, as shown in Figure 3. The PA gain curve remains flat for input powers below the breakpoint level, and begins to compress at a given rate (slope) for input powers greater than the breakpoint level. To compensate for such gain compression, the MAX2010 generates a gain expansion, which occurs at the same breakpoint level with the opposite slope. The overall result is a flat gain response at the PA output.

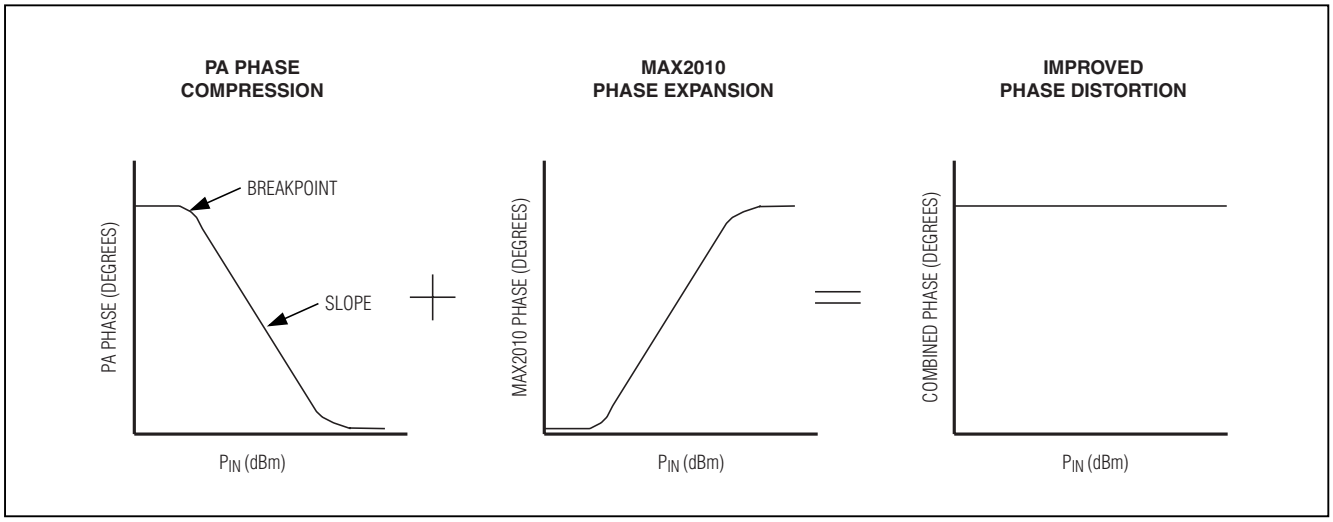


Figure 1. PA Phase Compression Canceled by MAX2010 Phase Expansion

500MHz to 1100MHz Adjustable RF Predistorter

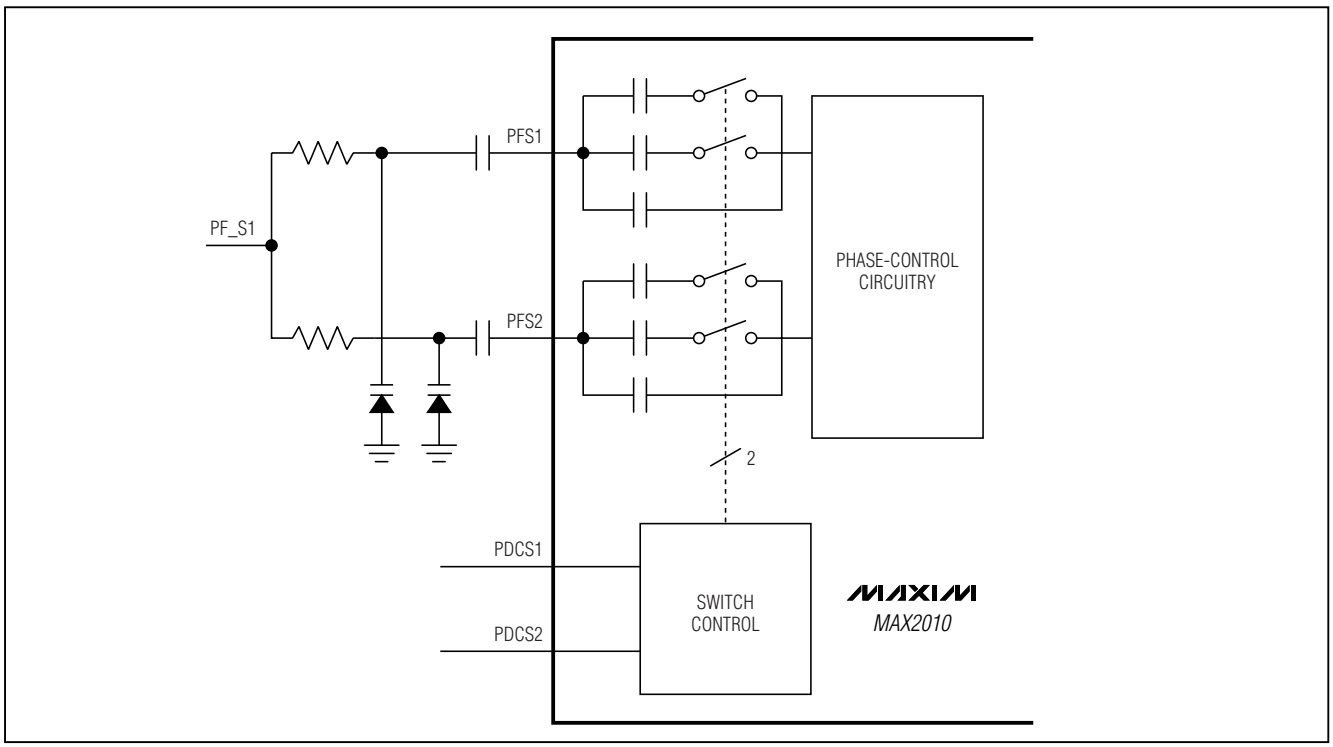


Figure 2. Simplified Phase Slope Internal Circuitry

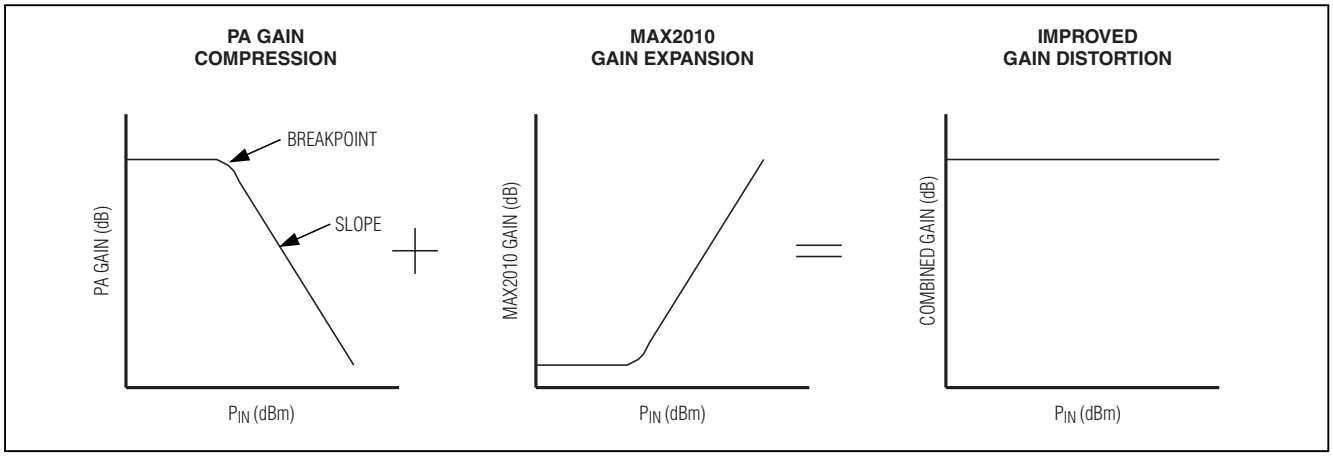


Figure 3. PA Gain Compression Canceled by MAX2010 Gain Expansion

Gain Expansion Breakpoint

The gain expansion breakpoint is usually controlled by a DAC connected through the GBP pin. The GBP input voltage range of 0.5V to 5V corresponds to a breakpoint input power range of -2.5dBm to 23dBm. To achieve the optimal performance, the gain expansion breakpoint of the MAX2010 must be set to equal the gain compression point of the PA. The GBP control has a minimal effect on the small-signal gain when operated from 0.5V to 5V.

Gain Expansion Slope

In addition to properly setting the breakpoint, the gain expansion slope of the MAX2010 must also be adjusted to compensate for the PA's gain compression. The slope should be set using the following equation:

$$MAX2010\_SLOPE = \frac{-PA\_SLOPE}{1+PA\_SLOPE}$$

where:

MAX2010_SLOPE = MAX2010 gain section's slope in dB/dB.

PA_SLOPE = PA's gain slope in dB/dB, a negative number for compressive behavior.

To modify the gain expansion slope, two adjustments must be made to the biases applied on pins GCS and GFS. Both GCS and GFS have an input voltage range of 0V to V_{CC}, corresponding to a slope of approximately 0.1dB/dB to 0.53dB/dB. The slope is set to maximum when V_{GCS} = 0V and V_{GFS} = +5V, and the slope is at its minimum when V_{GCS} = +5V and V_{GFS} = 0V.

Unlike the GBP pin, modifying the gain expansion slope bias on the GCS pin causes a change in the part's insertion loss and noise figure. For example, a smaller slope caused by GCS results in a better insertion loss and lower noise figure. The GFS does not affect the insertion loss. It can provide up to -30% or +30% total slope variation around the nominal slope set by GCS.

Large amounts of GCS bias adjustment can also lead to an undesired (or residual) phase expansion/compression behavior. There exists an optimal bias voltage that minimizes this parasitic behavior (typically GCS = 1.0V). Control voltages higher than the optimal result in parasitic phase expansion, lower control voltages result in phase compression. GFS does not contribute to the phase behavior and is preferred for slope control.

Applications Information

The following section describes the tuning methodology best implemented with a class A amplifier. Other classes of operation may require significantly different settings.

Gain and Phase Expansion Optimization

The best approach to improve the ACPR of a PA is to first optimize the AM-PM response of the phase section. For most high-frequency LDMOS amplifiers, improving the AM-PM response provides the bulk of the ACPR improvement. Figure 4 shows a typical configuration of the phase tuning circuit. A power sweep on a network analyzer allows quick real-time tuning of the AM-PM response. First, tune PBIN to achieve the phase expansion starting point (breakpoint) at the same point where the PA's phase compression begins. Next, use control pins PF_S1, PDCS1, and PDCS2 to obtain the optimal AM-PM response. The typical values for these pins are shown in Figure 4.

To further improve the ACPR, connect the phase output to the gain input through a preamplifier. The preamplifier is used to compensate for the high insertion loss of the gain section. Figure 5 shows a typical application circuit of the MAX2010 with the phase section cascaded to the gain section for further ACPR optimization. Similar to tuning the phase section, first tune the gain expansion breakpoint through the GBP pin and adjust for the desired gain expansion with pins GCS and GFS. To minimize the effect of GCS on the parasitic phase response, minimize the control voltage to around 1V. Some retuning of the AM-PM response may be necessary.

Layout Considerations

A properly designed PC board is an essential part of any high-frequency circuit. In order to minimize external components, the PC board can be designed to incorporate small values of inductance and capacitance to optimize the input and output VSWR (refer to the MAX2009/MAX2010 EV Kit). The phase section's PFS1 and PFS2 pins are sensitive to external parasitics. Minimize trace lengths and keep varactor diodes close to the pins. Remove the ground plane underneath the traces can further help reduce the parasitic capacitance. For best performance, route the ground pin traces directly to the grounded EP underneath the package. Solder the EP on the bottom of the device package evenly to the board ground plane to provide a heat transfer path along with signal grounding.

500MHz to 1100MHz Adjustable RF Predistorter

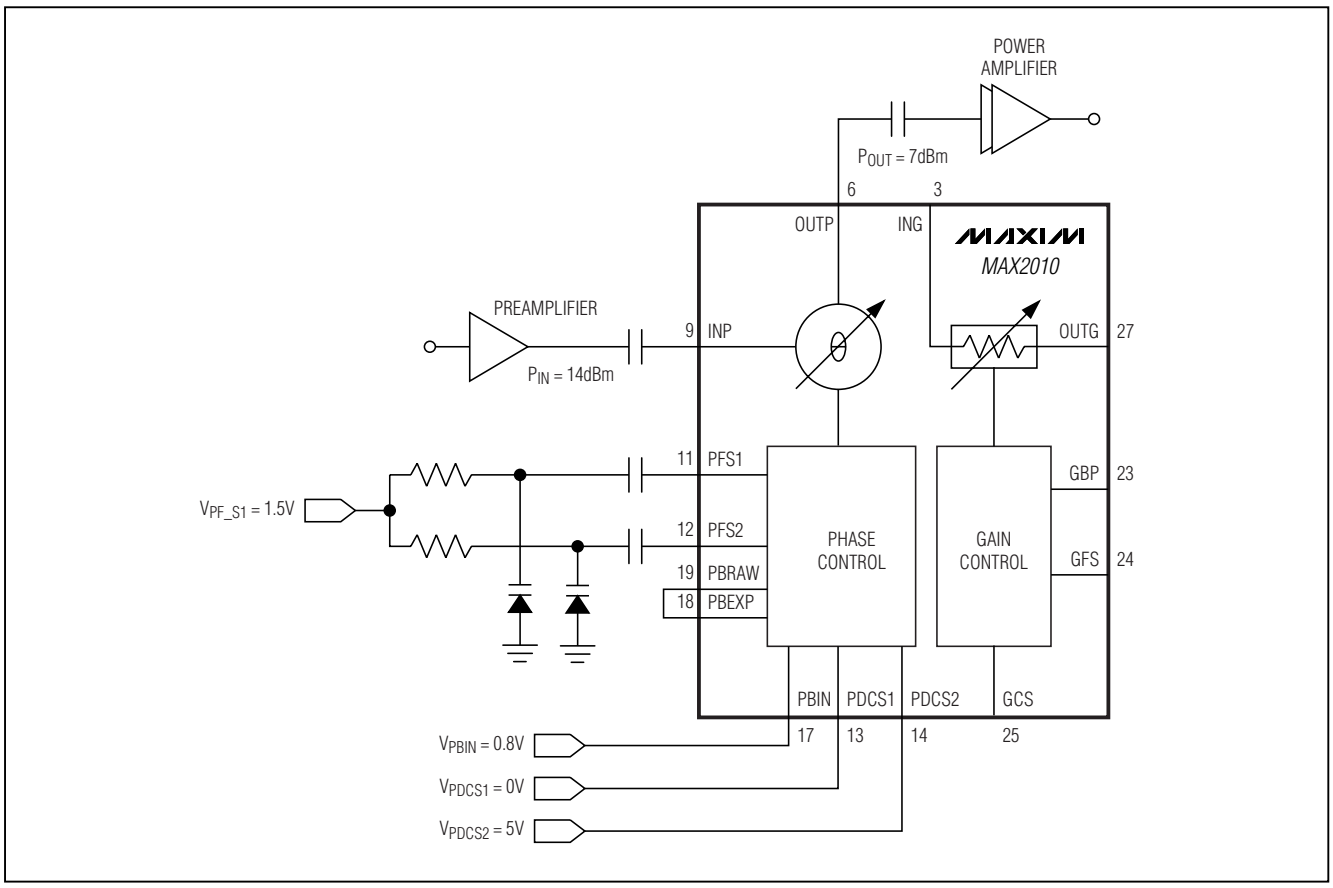


Figure 4. AM-PM Response Tuning Circuit

Power-Supply Bypassing

Bypass each V_{CC} pin with a 0.01µF capacitor.

Exposed Pad RF

The exposed paddle (EP) of the MAX2010's 28-pin thin QFN-EP package provides a low inductance path to ground. It is important that the EP be soldered to the ground plane on the PC board, either directly or through an array of plated via holes.

Table 1. Suggested Components of Typical Application Circuit

DESIGNATION	VALUE	TYPE
C1, C2, C3, C10	100pF ±5%	0402 ceramic capacitors
C4, C5	0.01µF ±10%	0603 ceramic capacitors
C6, C8	15pF ±5%	0402 ceramic capacitors
C11, C12	2.2pF ±0.1pF	0402 ceramic capacitors
L1, L2	5.6nH ±0.3nH	0402 ceramic inductors
R1, R2	1kΩ ±5%	0402 resistors
VR1, VR2	Skyworks SMV1232-079	Hyperabrupt varactor diodes

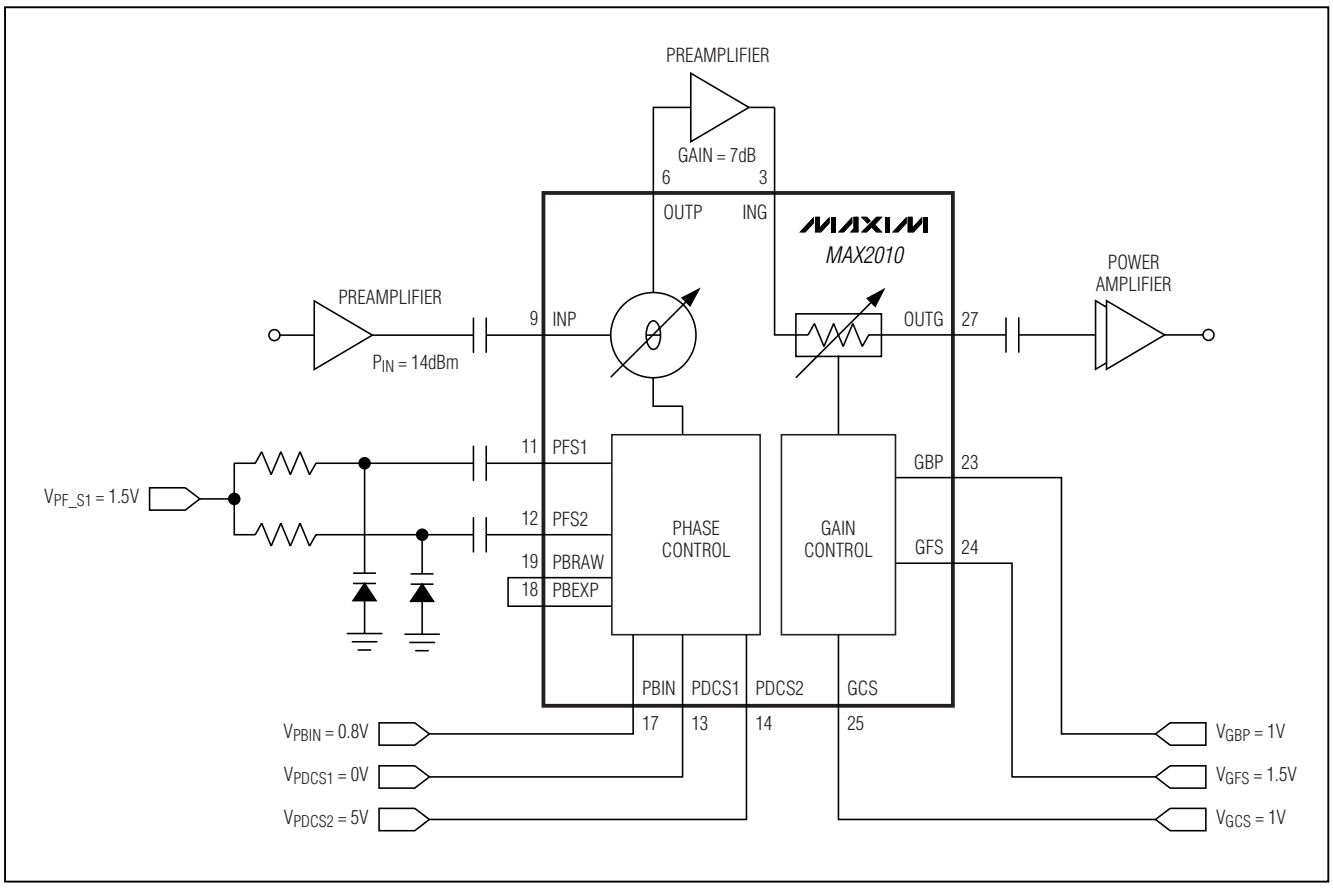


Figure 5. MAX2010 Phase and Gain Optimization Circuit

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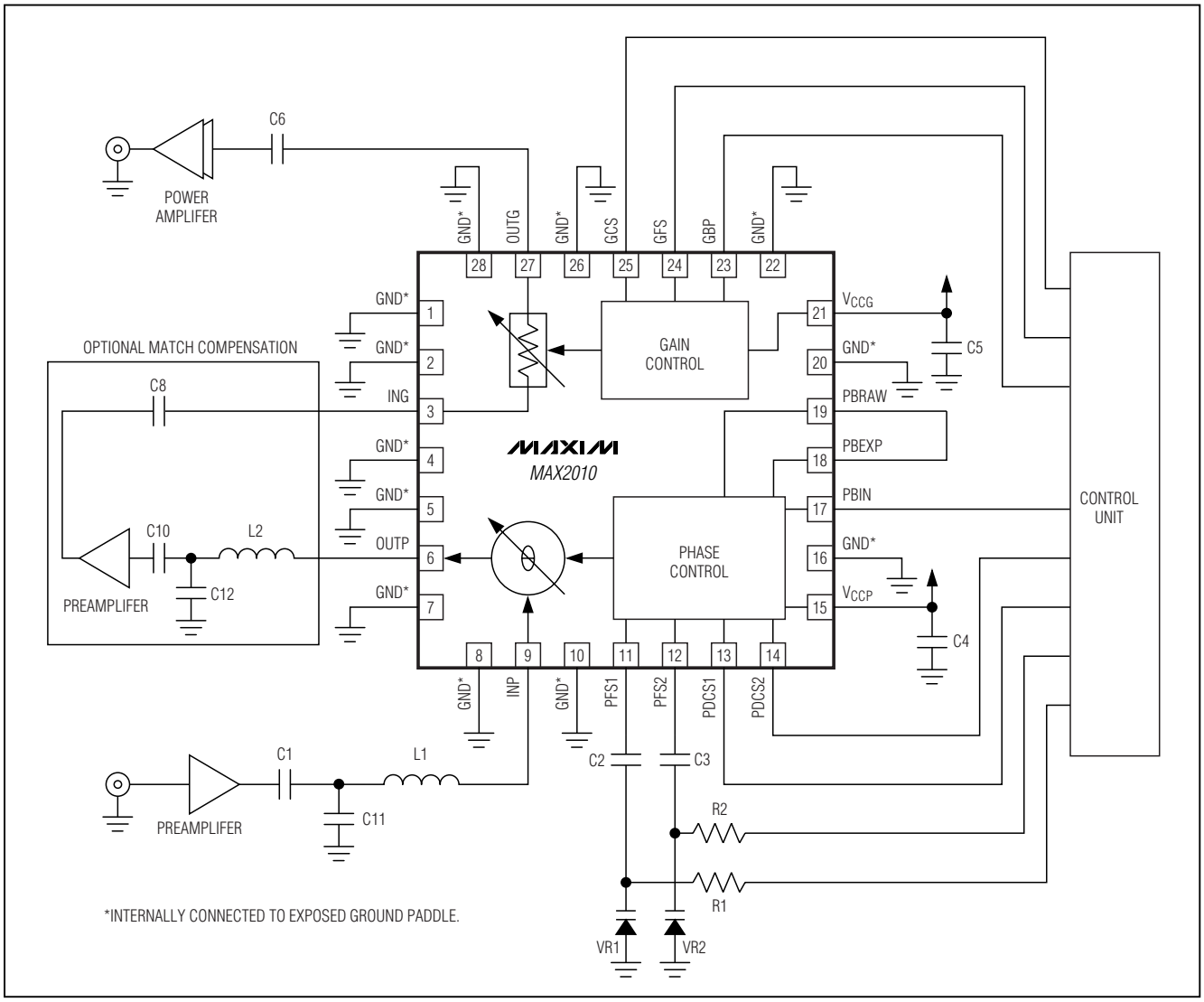
Typical Application Circuit



Chip Information

TRANSISTOR COUNT:

Bipolar: 160

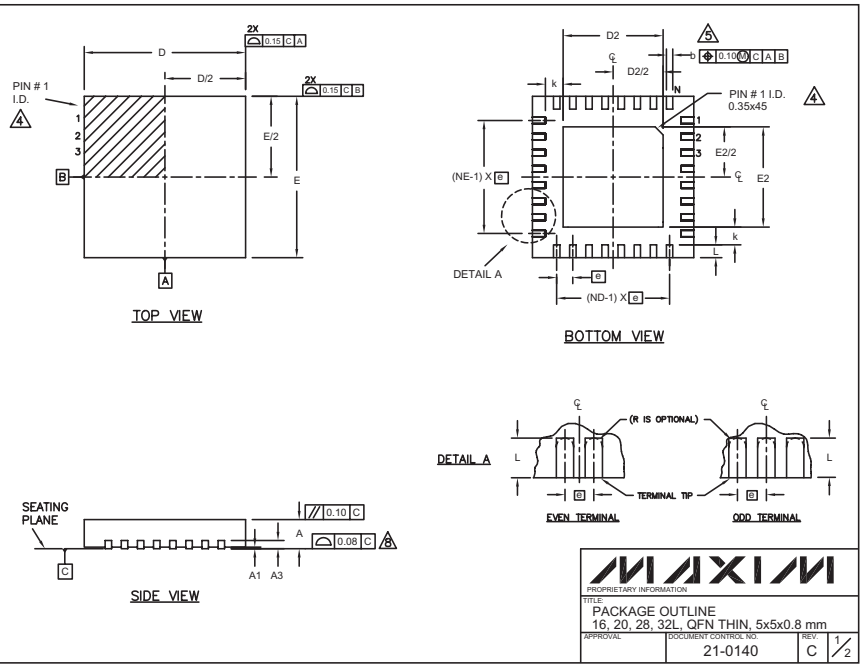
CMOS: 240

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE 16, 20, 28, 32L, QFN THIN, 5x5x0.8 mm

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COMMON DIMENSIONS

PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE 16, 20, 28, 32L, QFN THIN, 5x5x0.8 mm

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